DSP/BIOS HWI/SWI Example

**Start Below and Follow the Arrows**

SWI_vision calls its function visionswi(). Inside this function a connected parts algorithm is run and/or any other algorithm the user wishes to implement. After processing the image, it checks to see if Linux is ready to receive a new image for sending over the network. If the Linux_ready flag is set, EDMA is used to transfer the image to another buffer in memory allowing Linux to use as much time as needed to transfer the image. visionswi also checks if the Color_LCD_ready flag is set. If it is, the image is transferred to a second storage buffer allowing the LCD code to take as long as it needs to transfer the image to the color LCD.

**SWI Level**

HWI_INT4 is triggered when the VPIF is finished receiving and transferring to memory the 288 X 384 pixel image. The image is formatted in the Bayer pattern. HWI_INT4 pulls the PRU (Programmable Real-Time Unit) out of suspend to start the processing of the image.

**HWI Level**

PRU1’s job is to De-Mosaic the Bayer patterned image producing a 144 X 176 RGB image. In addition produces a 72 X 88 image. When it is finished it interrupts the DSP core.

**EDMA and PRU Level**

EDMA1_Channel31 transfers current 144 X 176 RGB image to a shared memory location that a Linux application can also access.

**Peripheral Level**

OMAPL138 VPIF (Video Port Interface)

OMAPL138 SPI Serial Port

SWI_lcd formats the 144 X 176 RGB 24 bit color image to a 12 bit color image formatted for the Color LCD. When it has completed converting all the pixels to 12 bit color it sets up the EDMA to transfer the image to the LCD over the SPI serial port.

**Peripheral Level**

Color Camera

VSYNC HREF PCLK 8 bit data bus

Color LCD

**Peripheral Level**

SPI_CS SPICLK SPI_SIMO

**EDMA Level**

EDMA1_Channel30 transfers current 144 X 176 RGB image to a memory location known also by the color LCD data transfer code.

**EDMA and PRU Level**

EDMA0_Channel19 transfers 12 bit color image to the Color LCD through the OMAPL138’s SPI serial port.

**HWI Level**

HWI_INT6 triggered by the PRU1. The image is ready for processing so post SWI SWI_vision.

**SWI Level**

HWI_INT5 for EDMA CH31 is triggered when the EDMA memory transfer is complete. This interrupt function simply flags Linux indicating a new image is ready to be read.

**SWI Level**

HWI_INT5 for EDMA CH30 is triggered when the EDMA memory transfer is complete. This interrupt function posts SWI SWI_lcd.

**SWI Level**

HWI_INT8 EDMA transfer through the SPI port to the Color LCD finished. Here simply set flag that indicates that the LCD is ready for another image.