SPI Timing Diagram  (MSB First) CLK POLARITY=0 and PHASE=1 on TMS320F28335

GND

MOSI

MISO

SCK

SS

x 10^-6
The selection procedure for the SPI clocking scheme is shown in Table 1-3. Examples of these four clocking schemes relative to transmitted and received data are shown in Figure 1-4.

Table 1-3. SPI Clocking Scheme Selection Guide

<table>
<thead>
<tr>
<th>SPICLK Scheme</th>
<th>CLOCK POLARITY (SPICCR.6)</th>
<th>CLOCK PHASE (SPICTL.3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rising edge without delay</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Rising edge with delay</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Falling edge without delay</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Falling edge with delay</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 1-4. SPICLK Signal Options

For the SPI, SPICLK symmetry is retained only when the result of (SPIBRR+1) is an even value. When (SPIBRR + 1) is an odd value and SPIBRR is greater than 3, SPICLK becomes asymmetrical. The low pulse of SPICLK is one CLKOUT longer than the high pulse when the CLOCK POLARITY bit is clear (0). When the CLOCK POLARITY bit is set to 1, the high pulse of the SPICLK is one CLKOUT longer than the low pulse, as shown in Figure 1-5.

Figure 1-5. SPI: SPICLK-CLKOUT Characteristic When (BRR + 1) is Odd, BRR > 3, and CLOCK POLARITY = 1

Note: Previous data bit
I2C Timing Diagram (MSB First) (Red indicates when slave has control of SDA)

Start is High-Low on SDA when SCL High
Stop is Low-High on SDA when SCL High

0111100W 00001110 10101100 00011111

I2C Timing Diagram (MSB First) (Red indicates when slave has control of SDA)

Start is High-Low on SDA when SCL High
Stop is Low-High on SDA when SCL High

0111100R 00000101 00010111 11011101

3.3V
SCL
GND

Start
SDA
GND

3.3V
SCL
GND

Start
SDA
GND

x 10^-4

Start
Click here to view full image.

Stop
Click here to view full image.

Stop
Click here to view full image.