Digital I/O Cheat Sheet

Port 1

P1IN.7	P1IN.6	P1IN.5	P1IN.4	P1IN.3	P1IN.2	P1IN.1	P1IN.0

P1OUT.7	P1OUT.6	P1OUT.5	P1OUT.4	P1OUT.3	P1OUT.2	P1OUT.1	P1OUT.0

P1DIR.7	P1DIR.6	P1DIR.5	P1DIR.4	P1DIR.3	P1DIR.2	P1DIR.1	P1DIR.0

P1REN.7	P1REN.6	P1REN.5	P1REN.4	P1REN.3	P1REN.2	P1REN.1	P1REN.0

P1SEL.7	P1SEL.6	P1SEL.5	P1SEL.4	P1SEL.3	P1SEL.2	P1SEL.1	P1SEL.0

P1IFG.7	P1IFG.6	P1IFG.5	P1IFG.4	P1IFG.3	P1IFG.2	P1IFG.1	P1IFG.0

P1IES.7	P1IES.6	P1IES.5	P1IES.4	P1IES.3	P1IES.2	P1IES.1	P1IES.0

P1IE.7	P1IE.6	P1IE.5	P1IE.4	P1IE.3	P1IE.2	P1IE.1	P1IE.0

Table 21. Port P1 (P1.0 to P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK/ADC10CLK	0	P1.0(1)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		ADC10CLK	1	1
P1.1/TA0	1	P1.1(1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2(1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TA2	3	P1.3(1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1

(1) Default after reset (PUC/POR)

Table 22. Port P1 (P1.4 to P1.6) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.4/SMCLK/TCK	4	P1.4(2) (I/O)	I: 0; O: 1	0	0
		SMCLK	1	1	0
		TCK	X	X	1
P1.5/TA0/TMS	5	P1.5(2) (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA0	1	1	0
		TMS	X	X	1
P1.6/TA1/TDI/TCLK	6	P1.6(2) (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA1	1	1	0
		TDI/TCLK(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Function controlled by JTAG

Table 23. Port P1 (P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.7/TA2/TDO/TDI	7	P1.7(2) (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA2	1	1	0
		TDO/TDI(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Function controlled by JTAG

Port 2

P2IN.7	P2IN.6	P2IN.5	P2IN.4	P2IN.3	P2IN.2	P2IN.1	P2IN.0

P2OUT.7	P2OUT.6	P2OUT.5	P2OUT.4	P2OUT.3	P2OUT.2	P2OUT.1	P2OUT.0

P2DIR.7	P2DIR.6	P2DIR.5	P2DIR.4	P2DIR.3	P2DIR.2	P2DIR.1	P2DIR.0

P2REN.7	P2REN.6	P2REN.5	P2REN.4	P2REN.3	P2REN.2	P2REN.1	P2REN.0

P2SEL.7	P2SEL.6	P2SEL.5	P2SEL.4	P2SEL.3	P2SEL.2	P2SEL.1	P2SEL.0

P2IFG.7	P2IFG.6	P2IFG.5	P2IFG.4	P2IFG.3	P2IFG.2	P2IFG.1	P2IFG.0

P2IES.7	P2IES.6	P2IES.5	P2IES.4	P2IES.3	P2IES.2	P2IES.1	P2IES.0

P2IE.7	P2IE.6	P2IE.5	P2IE.4	P2IE.3	P2IE.2	P2IE.1	P2IE.0

Table 24. Port P2 (P2.0, P2.2) Pin Functions

Pin Name (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS[1]		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.0/ACLK/A0/OA0I0	0	0	P2.0[2] (I/O)	I: 0; O: 1	0	0
			ACLK	1	1	0
			A0/OA0I0[3]	X	X	1
P2.2/TA0/A2/OA0I1	2	2	P2.2[2] (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI0B	0	1	0
			Timer_A3.TA0	1	1	0
			A2/OA0I1[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Table 25. Port P2 (P2.1) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS[1]		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.1/TAINCLK/SMCLK/ A1/OA0O	1	1	P2.1[2] (I/O)	I: 0; O: 1	0	0
			Timer_A3.INCLK	0	1	0
			SMCLK	1	1	0
			A1/OA0O[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Table 26. Port P2 (P2.3) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS[1]		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.3/TA1/A3/V_{REF-} /V_{eREF-}/ OA1I1/OA1O	3	3	P2.3[2] (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI1B	0	1	0
			Timer_A3.TA1	1	1	0
			A3/V_{REF-}/V_{eREF-}/OA1I1/OA1O[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Table 27. Port P2 (P2.4) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS[1]		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.4/TA2/A4/V_{REF+}/ V_{eREF+}/ OA1I0	4	4	P2.4[2] (I/O)	I: 0; O: 1	0	0
			Timer_A3.TA2	1	1	0
			A4/V_{REF+}/V_{eREF+}/OA1I0[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Table 28. Port P2 (P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P2DIR.x	P2SEL.x	DCOR
P2.5/R_{OSC}	5	P2.5[2] (I/O)	I: 0; O: 1	0	0
		N/A[3]	0	1	0
		DV_{SS}	1	1	0
		R_{OSC}	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) N/A = Not available or not applicable

Table 29. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]	
			P2DIR.x	P2SEL.x
P2.6/XIN	6	P2.6 (I/O)	I: 0; O: 1	0
		XIN[2]	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)

Table 30. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]	
			P2DIR.x	P2SEL.x
XOUT/P2.7	7	P2.7 (I/O)	I: 0; O: 1	0
		XOUT[2] [3]	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) If the pin XOUT/P2.7 is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

Port 3

P3IN.7	P3IN.6	P3IN.5	P3IN.4	P3IN.3	P3IN.2	P3IN.1	P3IN.0

P3OUT.7	P3OUT.6	P3OUT.5	P3OUT.4	P3OUT.3	P3OUT.2	P3OUT.1	P3OUT.0

P3DIR.7	P3DIR.6	P3DIR.5	P3DIR.4	P3DIR.3	P3DIR.2	P3DIR.1	P3DIR.0

P3REN.7	P3REN.6	P3REN.5	P3REN.4	P3REN.3	P3REN.2	P3REN.1	P3REN.0

P3SEL.7	P3SEL.6	P3SEL.5	P3SEL.4	P3SEL.3	P3SEL.2	P3SEL.1	P3SEL.0

Table 31. Port P3 (P3.0) Pin Functions

PIN NAME (P1.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS(1)		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.0/UCB0STE/ UCA0CLK/A5	0	5	P3.0(2) (I/O)	I: 0; O: 1	0	0
			UCB0STE/UCA0CLK(3) (4)	X	1	0
			A5(5)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) The pin direction is controlled by the USCI module.
(4) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(5) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Table 32. Port P3 (P3.1 to P3.5) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)	
			P3DIR.x	P3SEL.x
P3.1/UCB0SIMO/UCB0SDA	1	P3.1(2) (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA(3)	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2(2) (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL(3)	X	1
P3.3/UCB0CLK/UCA0STE	3	P3.3(2) (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE(3) (4)	X	1
P3.4/UCA0TXD/UCA0SIMO	4	P3.4(2) (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO(3)	X	1
P3.5/UCA0RXD/UCA0SOMI	5	P3.5(2) (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI(3)	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) The pin direction is controlled by the USCI module.
(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode even if 4-wire SPI mode is selected.

Table 33. Port P3 (P3.6, P3.7) Pin Functions

PIN NAME (P3.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS(1)		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.6/A6/OA0I2	6	6	P3.6(2) (I/O)	I: 0; O: 1	0	0
			A6/OA0I2(3)	X	X	1
P3.7/A7/OA1I2	7	7	P3.7(2) (I/O)	I: 0; O: 1	0	0
			A7/OA1I2(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port 4

P4IN.7	P4IN.6	P4IN.5	P4IN.4	P4IN.3	P4IN.2	P4IN.1	P4IN.0

P4OUT.7	P4OUT.6	P4OUT.5	P4OUT.4	P4OUT.3	P4OUT.2	P4OUT.1	P4OUT.0

P4DIR.7	P4DIR.6	P4DIR.5	P4DIR.4	P4DIR.3	P4DIR.2	P4DIR.1	P4DIR.0

P4REN.7	P4REN.6	P4REN.5	P4REN.4	P4REN.3	P4REN.2	P4REN.1	P4REN.0

P4SEL.7	P4SEL.6	P4SEL.5	P4SEL.4	P4SEL.3	P4SEL.2	P4SEL.1	P4SEL.0

Table 34. Port P4 (P4.0 to P4.2) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0(1) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI0A	0	1
		Timer_B3.TB0	1	1
P4.1/TB1	1	P4.1(1) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.TB1	1	1
P4.2/TB2	2	P4.2(1) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI2A	0	1
		Timer_B3.TB2	1	1

(1) Default after reset (PUC/POR)

Table 35. Port P4 (P4.3 to P4.4) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS(1)		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.3/TB0/A12/OA0O	3	4	P4.3(2) (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI0B	0	1	0
			Timer_B3.TB0	1	1	0
			A12/OA0O(3)	X	X	1
P4.4/TB1/A13/OA1O	4	5	P4.4(2) (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI1B	0	1	0
			Timer_B3.TB1	1	1	0
			A13/OA1O(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Table 36. Port P4 (P4.5) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS(1)		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.5/TB3/A14/OA0I3	5	6	P4.5(2) (I/O)	I: 0; O: 1	0	0
			Timer_B3.TB2	1	1	0
			A14/OA0I3(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Table 37. Port P4 (P4.6) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS(1)		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.6/TBOUTH/A15/OA1I3	6	7	P4.6(2) (I/O)	I: 0; O: 1	0	0
			TBOUTH	0	1	0
			DV_{SS}	1	1	0
			A15/OA1I3(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Table 38. Port P4 (Pr.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.7/TBCLK	7	P4.7(1) (I/O)	I: 0; O: 1	0
		Timer_B3.TBCLK	0	1
		DV_{SS}	1	1

(1) Default after reset (PUC/POR)