## Timer_A3 Cheat Sheet

### TACTL

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<th>15</th>
<th>14</th>
<th>13</th>
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<td>Unused</td>
<td>TASSELx</td>
<td>IDx</td>
<td>MCx</td>
<td>Unused</td>
<td>TACLR</td>
<td>TAIE</td>
<td>TAIFG</td>
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- **TASSELx**
  - Bits 15-10: Timer_A clock source select
    - 00: TACLK
    - 01: ACLK
    - 10: SMCLK
    - 11: INCLK (INCLK is device-specific and is often assigned to the internal TCLK (TACLK)) (see the device-specific data sheet)

- **IDx**
  - Bits 7-4: Input divider. These bits select the divider for the input clock.
    - 00: 1
    - 01: 2
    - 10: 4
    - 11: 8

- **MCx**
  - Bits 5-4: Mode control. Setting MCx = 00h when Timer_A is not in use conserves power.
    - 00: Stop mode: the timer is halted.
    - 01: Up mode: the timer counts up to TACCRO.
    - 10: Continuous mode: the timer counts up to 0FFFFh.
    - 11: Up/down mode: the timer counts up to TACCRO then down to 0000h.

- **Unused**
  - Bit 3: Unused

- **TACLR**
  - Bit 2: Timer_A clear. Setting this bit resets TAR, the clock divider, and the count direction. The TACLR bit is automatically reset and is always read as zero.

- **TAIE**
  - Bit 1: Timer_A interrupt enable. This bit enables the TAIFG interrupt request.
    - 0: Interrupt disabled
    - 1: Interrupt enabled

- **TAIFG**
  - Bit 0: Timer_A interrupt flag
    - 0: No interrupt pending
    - 1: Interrupt pending

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**The TAR is the count of Timer_A**

### TACCRx same for TACCR0, TACCR1, TACCR2

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- **Timer_Ax capture/compare register**
  - **Compare mode:** TACCRx holds the value for the comparison to the timer value in TARx
  - **Capture mode:** The Timer_Ax Register, TAR, is copied into the TACCRx register when a capture event occurs
### TACCTLx same for TACCTL0, TACCTL1 and TACCTL2

| Bit 15-14 | Capture mode  
|------------|---------------|
| 00 | No capture  
| 01 | Capture on rising edge  
| 10 | Capture on falling edge  
| 11 | Capture on both rising and falling edges  

### CCISx Bit 13-12 Carccept/compare input select. These bits select the TACCx input signal. See the device-specific data sheet for specific signal connections.  
| Bit 11-10 | Capture/compare select. The selected CCI input signal is latched with the EQUx signal and can be read via this bit  
| 00 | Capture mode  
| 01 | Capture mode  
| 10 | Capture mode  
| 11 | Capture mode  

### SCS Bit 11 Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock.  
| Bit 10-9 | Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock.  
| 00 | Synchronize capture source  
| 01 | Synchronize capture source  
| 10 | Synchronize capture source  
| 11 | Synchronize capture source  

###CCI Bit 10 Synchronize capture/compare input. The selected CCI input signal is latched with the EQUx signal and can be read via this bit  
| Bit 9-8 | Capture mode  
| 00 | Capture mode  
| 01 | Capture mode  
| 10 | Capture mode  
| 11 | Capture mode  

### OUTMODx Bits 7-5 Output mode. Modes 2, 3, 6, and 7 are not useful for TACCR0, because EQUx = EQU0  
| Bit 4-3 | Output mode  
| 00 | Output mode  
| 01 | Output mode  
| 10 | Output mode  
| 11 | Output mode  

### CCIE Bit 4 Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag.  
| Bit 3-2 | Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag.  
| 00 | Capture/compare interrupt enabled  
| 01 | Capture/compare interrupt enabled  
| 10 | Capture/compare interrupt enabled  
| 11 | Capture/compare interrupt enabled  

### OUT Bit 2 Output. For output mode 0, this bit directly controls the state of the output.  
| Bit 1-0 | Output mode. For output mode 0, this bit directly controls the state of the output.  
| 00 | Output low  
| 01 | Output high  
| 10 | Output high  
| 11 | Output high  

### CCIFG Bit 0 Capture/compare interrupt flag  
| Bit 0 | Capture/compare interrupt flag  
| 00 | Capture/compare interrupt flag  
| 01 | Capture/compare interrupt flag  

### TAIx Bit 15-0 Timer_A interrupt vector value  
| TAIx | Bits 15-0  
| 00 | Timer_A interrupt vector value  

### TAIx Interrupt Source  
| TAIx | Interrupt Source  
| 0000 | No interrupt pending  
| 0001 | Capture/compare 1  
| 0010 | Capture/compare 2  
| 0011 | Reserved  
| 0100 | Reserved  
| 0101 | Timer overflow  
| 0110 | Reserved  
| 0111 | Reserved  

### TAIx Interrupt Priority  
| TAIx | Interrupt Priority  
| 0000 | Highest  
| 0001 | Highest  
| 0010 | Highest  
| 0011 | Highest  
| 0100 | Lowest  
| 0101 | Lowest  
| 0110 | Lowest  
| 0111 | Lowest  

### TAIV Bit 15-0  
| TAIV | Bits 15-0  
| 0000 | TAIV  

### TAIVx Bit 15-0  
| TAIVx | Bits 15-0  
| 0000 | TAIVx  

### TAIVx Interrupt Source  
| TAIVx | Interrupt Source  
| 0000 | No interrupt pending  
| 0001 | Capture/compare 1  
| 0010 | Capture/compare 2  
| 0011 | Reserved  
| 0100 | Reserved  
| 0101 | Timer overflow  
| 0110 | Reserved  
| 0111 | Reserved  

### TAIVx Interrupt Priority  
| TAIVx | Interrupt Priority  
| 0000 | Highest  
| 0001 | Highest  
| 0010 | Highest  
| 0011 | Highest  
| 0100 | Lowest  
| 0101 | Lowest  
| 0110 | Lowest  
| 0111 | Lowest  

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**Notes:**
- **SCS**: Synchronize capture source.
- **CCI**: Capture/compare input select.
- **OUTMODx**: Output mode.
- **CCIE**: Capture/compare interrupt enable.
- **OUT**: Output mode.
- **CCIFG**: Capture/compare interrupt flag.
- **TAIV**: Timer_A interrupt vector value.
- **TAIVx**: Timer_A interrupt vector value.