

## Timer\_A3 Cheat Sheet

### TACTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Unused	Unused	Unused	Unused	Unused	Unused	TASSELx		IDx		MCx		Unused	TACLR	TAIE	TAIFG

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- Unused** Bits 15-10 **Unused**
- TASSELx** Bits 9-8 Timer\_A clock source select
  - 00 TACLK
  - 01 ACLK
  - 10 SMCLK
  - 11 INCLK (INCLK is device-specific and is often assigned to the inverted TBCLK) (see the device-specific data sheet)
- IDx** Bits 7-6 Input divider. These bits select the divider for the input clock.
  - 00 /1
  - 01 /2
  - 10 /4
  - 11 /8
- MCx** Bits 5-4 Mode control. Setting MCx = 00h when Timer\_A is not in use conserves power.
  - 00 Stop mode: the timer is halted.
  - 01 Up mode: the timer counts up to TACCR0.
  - 10 Continuous mode: the timer counts up to 0FFFFh.
  - 11 Up/down mode: the timer counts up to TACCR0 then down to 0000h.
- Unused** Bit 3 **Unused**
- TACLR** Bit 2 Timer\_A clear. Setting this bit resets TAR, the clock divider, and the count direction. The TACLR bit is automatically reset and is always read as zero.
- TAIE** Bit 1 Timer\_A interrupt enable. This bit enables the TAIFG interrupt request.
  - 0 Interrupt disabled
  - 1 Interrupt enabled
- TAIFG** Bit 0 Timer\_A interrupt flag
  - 0 No interrupt pending
  - 1 Interrupt pending

### TAR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The TAR is the count of Timer\_A

### TACCRx same for TACCR0, TACCR1, TACCR2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Timer\_Ax capture/compare register

Compare mode: TACCRx holds the value for the comparison to the timer value in TARx

Capture mode: The Timer\_Ax Register, TAR, is copied into the TACCRx register when a capture event occurs

TACCTLx same for TACCTL0, TACCTL1 and TACCTL2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMx		CCISx		SCS	SCCI	Unused	CAP	OUTMODx			CCIE	CCI	OUT	COV	CCIFG

- CMx** Bit 15-14 Capture mode
  - 00 No capture
  - 01 Capture on rising edge
  - 10 Capture on falling edge
  - 11 Capture on both rising and falling edges
- CCISx** Bit 13-12 Capture/compare input select. These bits select the TACCRx input signal. See the device-specific data sheet for specific signal connections.
  - 00 CClxA
  - 01 CClxB
  - 10 GND
  - 11 V<sub>CC</sub>
- SCS** Bit 11 Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock.
  - 0 Asynchronous capture
  - 1 Synchronous capture
- SCCI** Bit 10 Synchronized capture/compare input. The selected CCI input signal is latched with the EQUx signal and can be read via this bit.
- Unused** Bit 9 Unused. Read only. Always read as 0.
- CAP** Bit 8 Capture mode
  - 0 Compare mode
  - 1 Capture mode
- OUTMODx** Bits 7-5 Output mode. Modes 2, 3, 6, and 7 are not useful for TACCR0, because EQUx = EQU0.
  - 000 OUT bit value
  - 001 Set
  - 010 Toggle/reset
  - 011 Set/reset
  - 100 Toggle
  - 101 Reset
  - 110 Toggle/set
  - 111 Reset/set
- CCIE** Bit 4 Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag.
  - 0 Interrupt disabled
  - 1 Interrupt enabled
- CCI** Bit 3 Capture/compare input. The selected input signal can be read by this bit.
- OUT** Bit 2 Output. For output mode 0, this bit directly controls the state of the output.
  - 0 Output low
  - 1 Output high
- COV** Bit 1 Capture overflow. This bit indicates a capture overflow occurred. COV must be reset with software.
  - 0 No capture overflow occurred
  - 1 Capture overflow occurred
- CCIFG** Bit 0 Capture/compare interrupt flag
  - 0 No interrupt pending
  - 1 Interrupt pending

TAIV

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TAIV			0

**TAIVx** Bits 15-0 Timer\_A interrupt vector value

TAIV Contents	Interrupt Source	Interrupt Flag	Interrupt Priority
00h	No interrupt pending	-	
02h	Capture/compare 1	TACCR1 CCIFG	Highest
04h	Capture/compare 2 <sup>(1)</sup>	TACCR2 CCIFG	
08h	Reserved	-	
08h	Reserved	-	
0Ah	Timer overflow	TAIFG	
0Ch	Reserved	-	
0Eh	Reserved	-	Lowest