

## Timer\_B3 Cheat Sheet

### TBCTL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Unused</b>	<b>TBCLGRPx</b>		<b>CNTLx</b>		<b>Unused</b>	<b>TBSSELx</b>		<b>IDx</b>		<b>MCx</b>		<b>Unused</b>	<b>TBCLR</b>	<b>TBIE</b>	<b>TBIFG</b>	

<b>Unused</b>	Bit 15	<b>Unused</b>
<b>TBCLGRP</b>	Bit 14-13	<b>TBCLx group</b> 00 Each TBCLx latch loads independently 01 TBCL1+TBCL2 (TBCCR1 CLLDx bits control the update) TBCL3+TBCL4 (TBCCR3 CLLDx bits control the update) TBCL5+TBCL6 (TBCCR5 CLLDx bits control the update) TBCL0 independent 10 TBCL1+TBCL2+TBCL3 (TBCCR1 CLLDx bits control the update) TBCL4+TBCL5+TBCL6 (TBCCR4 CLLDx bits control the update) TBCL0 independent 11 TBCL0+TBCL1+TBCL2+TBCL3+TBCL4+TBCL5+TBCL6 (TBCCR1 CLLDx bits control the update)
<b>CNTLx</b>	Bits 12-11	<b>Counter length</b> 00 16-bit, TBR(max) = 0FFFFh 01 12-bit, TBR(max) = 0FFFh 10 10-bit, TBR(max) = 03FFh 11 8-bit, TBR(max) = 0FFh
<b>Unused</b>	Bit 10	<b>Unused</b>
<b>TBSSELx</b>	Bits 9-8	<b>Timer_B clock source select.</b> 00 TBCLK 01 ACLK 10 SMCLK 11 INCLK (INCLK is device-specific and is often assigned to the inverted TBCLK) (see the device-specific data sheet)
<b>IDx</b>	Bits 7-6	<b>Input divider. These bits select the divider for the input clock. 00 /101 /210 /411 /8</b>
<b>MCx</b>	Bits 5-4	<b>Mode control. Setting MCx = 00h when Timer_B is not in use conserves power.</b> 00 Stop mode: the timer is halted 01 Up mode: the timer counts up to TBCL0 10 Continuous mode: the timer counts up to the value set by CNTLx 11 Up/down mode: the timer counts up to TBCL0 and down to 0000h
<b>Unused</b>	Bit 3	<b>Unused</b>
<b>TBCLR</b>	Bit 2	<b>Timer_B clear. Setting this bit resets TBR, the clock divider, and the count direction. The TBCLR bit is automatically reset and is always read as zero.</b>
<b>TBIE</b>	Bit 1	<b>Timer_B interrupt enable. This bit enables the TBIFG interrupt request.</b> 0 Interrupt disabled 1 Interrupt enabled
<b>TBIFG</b>	Bit 0	<b>Timer_B interrupt flag.</b> 0 No interrupt pending 1 Interrupt pending

### TBR

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The TBR is the count of Timer\_B

### TBCCRx same for TBCCR0, TBCCR1, TBCCR2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Timer\_Bx capture/compare register

Compare mode: TBCCRx is double buffered by the TBCLx compare latch. The TBCLx holds the value for the comparison to the timer value in TBRx

Capture mode: The Timer\_Bx Register, TBR, is copied into the TBCCRx register when a capture event occurs

TBCCTLx same for TBCCTL0, TBCCTL1 and TBCCTL2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMx		CCISx		SCS	CCLDx		CAP	OUTMODx			CCIE	CCI	OUT	COV	CCIFG

- CMx** Bit 15-14 Capture mode
  - 00 No capture
  - 01 Capture on rising edge
  - 10 Capture on falling edge
  - 11 Capture on both rising and falling edges
- CCISx** Bit 13-12 Capture/compare input select. These bits select the TBCCR<sub>x</sub> input signal. See the device-specific data sheet for specific signal connections.
  - 00 CCIxA
  - 01 CCIxB
  - 10 GND
  - 11 V<sub>CC</sub>
- SCS** Bit 11 Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock.
  - 0 Asynchronous capture
  - 1 Synchronous capture
- CCLDx** Bit 10-9 Compare latch load. These bits select the compare latch load event.
  - 00 TBCL<sub>x</sub> loads on write to TBCCR<sub>x</sub>
  - 01 TBCL<sub>x</sub> loads when TBR counts to 0
  - 10 TBCL<sub>x</sub> loads when TBR counts to 0 (up or continuous mode)
  - 11 TBCL<sub>x</sub> loads when TBR counts to TBCLD or to 0 (up/down mode)
- CAP** Bit 8 Capture mode
  - 0 Compare mode
  - 1 Capture mode
- OUTMODx** Bits 7-5 Output mode. Modes 2, 3, 6, and 7 are not useful for TBCL0 because EQU<sub>x</sub> = EQU0.
  - 000 OUT bit value
  - 001 Set
  - 010 Toggle/reset
  - 011 Set/reset
  - 100 Toggle
  - 101 Reset
  - 110 Toggle/set
  - 111 Reset/set
- CCIE** Bit 4 Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag.
  - 0 Interrupt disabled
  - 1 Interrupt enabled
- CCI** Bit 3 Capture/compare input. The selected input signal can be read by this bit.
- OUT** Bit 2 Output. For output mode 0, this bit directly controls the state of the output.
  - 0 Output low
  - 1 Output high
- COV** Bit 1 Capture overflow. This bit indicates a capture overflow occurred. COV must be reset with software.
  - 0 No capture overflow occurred
  - 1 Capture overflow occurred
- CCIFG** Bit 0 Capture/compare interrupt flag
  - 0 No interrupt pending
  - 1 Interrupt pending

TBIV

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0		TAIV		0

TBIVx Bits 15-0 Timer\_B interrupt vector value

TBIV Contents	Interrupt Source	Interrupt Flag	Interrupt Priority
00h	No interrupt pending	-	
02h	Capture/compare 1	TBCCR1 CCIFG	Highest
04h	Capture/compare 2	TBCCR2 CCIFG	
06h			
08h			
0Ah			
0Ch			
0Eh	Timer overflow	TBIFG	Lowest

Not on the MSP430F2272

(1) Not available on all devices