

USCI\_B0 Cheat Sheet

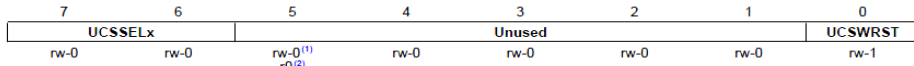
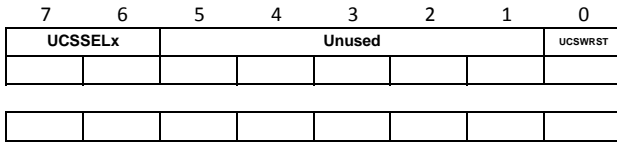
UCB0CTL0

7	6	5	4	3	2	1	0
UCCKPH	UCCKPL	UCMSB	UC7BIT	UCMST	UCMODEx		UCSYNC=1
							1
							1

7	6	5	4	3	2	1	0
UCCKPH	UCCKPL	UCMSB	UC7BIT	UCMST	UCMODEx		UCSYNC=1
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	

- UCCKPH** Bit 7 Clock phase select.
  - 0 Data is changed on the first UCLK edge and captured on the following edge.
  - 1 Data is captured on the first UCLK edge and changed on the following edge.
- UCCKPL** Bit 6 Clock polarity select.
  - 0 The inactive state is low.
  - 1 The inactive state is high.
- UCMSB** Bit 5 MSB first select. Controls the direction of the receive and transmit shift register.
  - 0 LSB first
  - 1 MSB first
- UC7BIT** Bit 4 Character length. Selects 7-bit or 8-bit character length.
  - 0 8-bit data
  - 1 7-bit data
- UCMST** Bit 3 Master mode select
  - 0 Slave mode
  - 1 Master mode
- UCMODEx** Bits 2-1 USCI mode. The UCMODEx bits select the synchronous mode when UCSYNC = 1.
  - 00 3-pin SPI
  - 01 4-pin SPI with UCxSTE active high: slave enabled when UCxSTE = 1
  - 10 4-pin SPI with UCxSTE active low: slave enabled when UCxSTE = 0
  - 11 I<sup>2</sup>C mode
- UCSYNC** Bit 0 Synchronous mode enable
  - 0 Asynchronous mode
  - 1 Synchronous mode

### UCB0CTL1



**UCSSELx** Bits 7-6 USCI clock source select. These bits select the BRCLK source clock in master mode. UCxCLK is always used in slave mode.

00	NA
01	ACLK
10	SMCLK
11	SMCLK

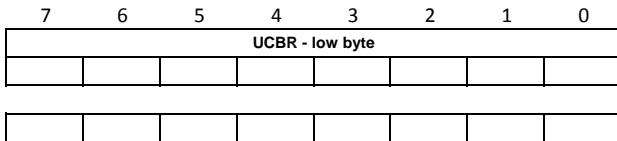
**Unused** Bits 5-1 Unused

**UCSWRST** Bit 0 Software reset enable

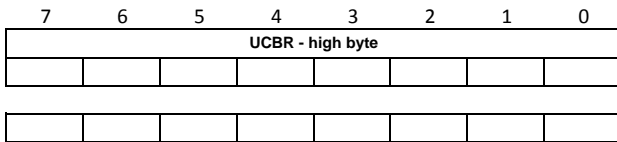
0	Disabled. USCI reset released for operation.
1	Enabled. USCI logic held in reset state.

<sup>(1)</sup> UCAxCTL1 (USCI\_Ax)  
<sup>(2)</sup> UCBxCTL1 (USCI\_Bx)

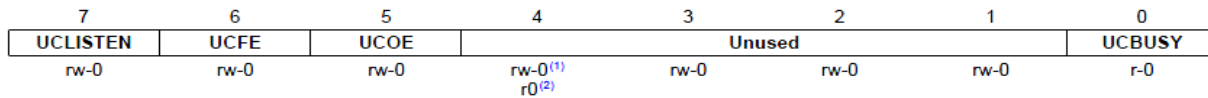
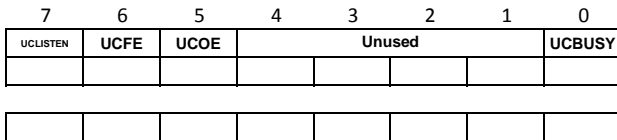
### UCBOBRO



### UCBOBR1



### UCB0STAT



**UCLISTEN** Bit 7 Listen enable. The UCLISTEN bit selects loopback mode.

0	Disabled
1	Enabled. The transmitter output is internally fed back to the receiver.

**UCFE** Bit 6 Framing error flag. This bit indicates a bus conflict in 4-wire master mode. UCFE is not used in 3-wire master or any slave mode.

0	No error
1	Bus conflict occurred

**UCOE** Bit 5 Overrun error flag. This bit is set when a character is transferred into UCxRXBUF before the previous character was read. UCOE is cleared automatically when UCxRXBUF is read, and must not be cleared by software. Otherwise, it will not function correctly.

0	No error
1	Overrun error occurred

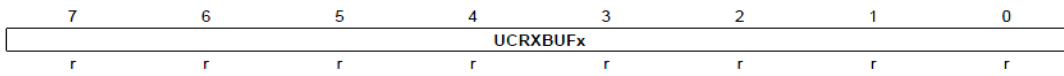
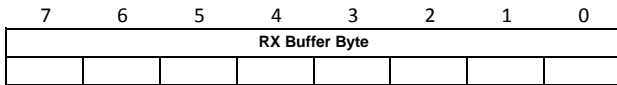
**Unused** Bits 4-1 Unused

**UCBUSY** Bit 0 USCI busy. This bit indicates if a transmit or receive operation is in progress.

0	USCI inactive
1	USCI transmitting or receiving

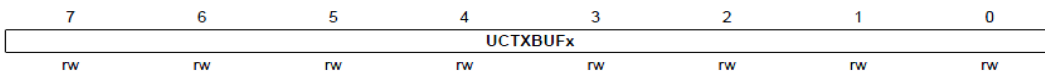
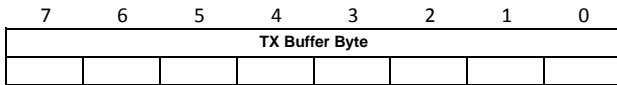
<sup>(1)</sup> UCAxSTAT (USCI\_Ax)  
<sup>(2)</sup> UCBxSTAT (USCI\_Bx)

### UCB0RXBUF



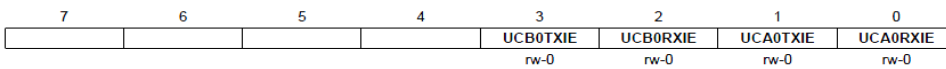
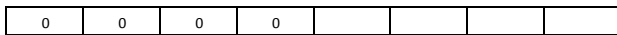
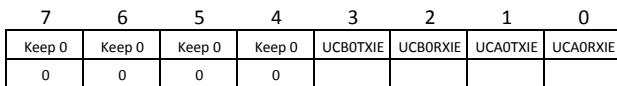
**UCRXBUFx** Bits 7-0 The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UCxRXBUF resets the receive-error bits, and UCxRXIFG. In 7-bit data mode, UCxRXBUF is LSB justified and the MSB is always reset.

### UCB0TXBUF



**UCTXBUFx** Bits 7-0 The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted. Writing to the transmit data buffer clears UCxTXIFG. The MSB of UCxTXBUF is not used for 7-bit data and is reset.

### IE2



**UCB0TXIE** Bits 7-4 These bits may be used by other modules (see the device-specific data sheet).

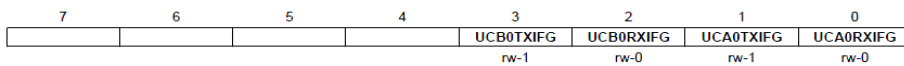
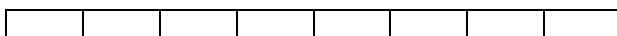
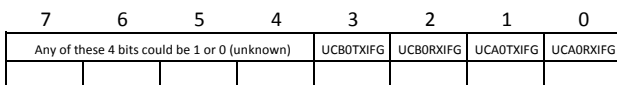
**UCB0TXIE** Bit 3 USCI\_B0 transmit interrupt enable  
 0 Interrupt disabled  
 1 Interrupt enabled

**UCB0RXIE** Bit 2 USCI\_B0 receive interrupt enable  
 0 Interrupt disabled  
 1 Interrupt enabled

**UCA0TXIE** Bit 1 USCI\_A0 transmit interrupt enable  
 0 Interrupt disabled  
 1 Interrupt enabled

**UCA0RXIE** Bit 0 USCI\_A0 receive interrupt enable  
 0 Interrupt disabled  
 1 Interrupt enabled

### IFG2



**UCB0TXIFG** Bits 7-4 These bits may be used by other modules (see the device-specific data sheet).

**UCB0TXIFG** Bit 3 USCI\_B0 transmit interrupt flag. UCB0TXIFG is set when UCB0TXBUF is empty.  
 0 No interrupt pending  
 1 Interrupt pending

**UCB0RXIFG** Bit 2 USCI\_B0 receive interrupt flag. UCB0RXIFG is set when UCB0RXBUF has received a complete character.  
 0 No interrupt pending  
 1 Interrupt pending

**UCA0TXIFG** Bit 1 USCI\_A0 transmit interrupt flag. UCA0TXIFG is set when UCA0TXBUF empty.  
 0 No interrupt pending  
 1 Interrupt pending

**UCA0RXIFG** Bit 0 USCI\_A0 receive interrupt flag. UCA0RXIFG is set when UCA0RXBUF has received a complete character.  
 0 No interrupt pending  
 1 Interrupt pending