16.3.6.1 Serial Clock Polarity and Phase

The polarity and phase of UCxCLK are independently configured via the UCCKPL and UCCKPH control bits of the USCI. Timing for each case is shown in Figure 16-4.

![USCI SPI Timing with UCMSB = 1](image-url)
### UCB0CTL1

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>UCSSELx</td>
<td>Unused</td>
<td>UCSWRISt</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **UCSSELx**: Bits 7-6. USCI clock source select. These bits select the BRCLK source clock in master mode. USCIxCLK is always used in slave mode.
  - 00: NA
  - 01: ACLK
  - 10: SMCLK
  - 11: SMCLK

- **UCSWRISt**: Bit 0. Software reset enable.
  - 0: Disabled. USCI reset released for operation.
  - 1: Enabled. USCI logic held in reset state.

---

### UCB0BR0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>UCBR - low byte</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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### UCB0BR1

<table>
<thead>
<tr>
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<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>UCBR - high byte</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

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### UCB0STAT

<table>
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<th>6</th>
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<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>UCLISTEN</td>
<td>UCFE</td>
<td>UCOE</td>
<td>Unused</td>
<td>UCBUSY</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **UCLISTEN**: Bit 7. Listen enable. The UCLISTEN bit selects loopback mode.
  - 0: Disabled
  - 1: Enabled. The transmitter output is internally fed back to the receiver.

- **UCFE**: Bit 6. Framing error flag. This bit indicates a bus conflict in 4-wire master mode. UCFE is not used in 3-wire master or any slave mode.
  - 0: No error
  - 1: Bus conflict occurred

- **UCOE**: Bit 5. Overrun error flag. This bit is set when a character is transferred into UCxRxBuf before the previous character was read. UCOE is cleared automatically when UCxRxBuf is read, and must not be cleared by software. Otherwise, it will not function correctly.
  - 0: No error
  - 1: Overrun error occurred

- **UCBUSY**: Bit 0. USCI busy. This bit indicates if a transmit or receive operation is in progress.
  - 0: USCI inactive
  - 1: USCI transmitting or receiving

---

- **UCAxSTAT (USCI_Ax)**
- **UCBxSTAT (USCI_Bx)**

---
UCBORXBUF

7 6 5 4 3 2 1 0

RX Buffer Byte

UCBRXBUF

7 6 5 4 3 2 1 0

UCBRXBUF contains the last received character from the receive shift register. Reading UCBRXBUF resets the receive-error bits, and UCBRXIFG. In 7-bit mode, UCBRXBUF is LSB justified and the MSB is always reset.

UCBOTXBUF

7 6 5 4 3 2 1 0

TX Buffer Byte

UCBTOXBUF

7 6 5 4 3 2 1 0

UCBTOXBUF is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted. Writing to the transmit data buffer clears UCBTOXIFG. The MSB of UCBTOXBUF is not used for 7-bit data and is reset.

IE2

7 6 5 4 3 2 1 0

Keep 0 Keep 0 Keep 0 Keep 0 UCBOTXIE UCBORXIE UCAOTXIE UCAORXIE

0 0 0 0

IE2 bits 7-4 These bits may be used by other modules (see the device-specific data sheet).

UCBOTXIE Bit 3 USCI_B0 transmit interrupt enable
0 Interrupt disabled
1 Interrupt enabled

UCBORXIE Bit 2 USCI_B0 receive interrupt enable
0 Interrupt disabled
1 Interrupt enabled

UCAOTXIE Bit 1 USCI_A0 transmit interrupt enable
0 Interrupt disabled
1 Interrupt enabled

UCAORXIE Bit 0 USCI_A0 receive interrupt enable
0 Interrupt disabled
1 Interrupt enabled

IFG2

7 6 5 4 3 2 1 0

Any of these 4 bits could be 1 or 0 (unknown) UCBOTXIFG UCBORXIFG UCAOTXIFG UCAORXIFG

IFG2 bits 7-4 These bits may be used by other modules (see the device-specific data sheet).

UCBOTHXIFG Bit 3 USCI_B0 transmit interrupt flag. UCBOTHXIFG is set when UCBOTXBUF is empty.
0 No interrupt pending
1 Interrupt pending

UCBORXIFG Bit 2 USCI_B0 receive interrupt flag. UCBORXIFG is set when UCBORXBUF has received a complete character.
0 No interrupt pending
1 Interrupt pending

UCAOTHXIFG Bit 1 USCI_A0 transmit interrupt flag. UCAOTHXIFG is set when UCAOTXBUF empty.
0 No interrupt pending
1 Interrupt pending

UCAORXIFG Bit 0 USCI_A0 receive interrupt flag. UCAORXIFG is set when UCAORXBUF has received a complete character.
0 No interrupt pending
1 Interrupt pending