# ADC10 Cheat Sheet

## ADC10CTL0 ADC10 Control Register 0

<table>
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<tr>
<th>Bit</th>
<th>Description</th>
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<td>15</td>
<td>SREFx</td>
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<tr>
<td>14</td>
<td>ADC10SHTx</td>
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<tr>
<td>13</td>
<td>ADC10SR</td>
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<td>12</td>
<td>REFOUT</td>
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<td>11</td>
<td>REFBURST</td>
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<td>10</td>
<td>MSC</td>
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<td>9</td>
<td>REF2_SV</td>
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<td>8</td>
<td>REFON</td>
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<td>7</td>
<td>ADC10ON</td>
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<td>ADC10IE</td>
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<td>5</td>
<td>ADC10IFG</td>
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<td>4</td>
<td>ENC</td>
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<tr>
<td>3</td>
<td>ADC10SC</td>
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</table>

### SREFx Bits 15-13
- Select reference.
- 000: \( V_{	ext{ref}} = V_{	ext{cc}} \) and \( V_{	ext{ref}} = V_{	ext{ss}} \)
- 001: \( V_{	ext{ref}} = V_{	ext{REF}}, \) and \( V_{	ext{ref}} = V_{	ext{ss}} \)
- 010: \( V_{	ext{ref}} = V_{	ext{REF}}, \) and \( V_{	ext{ref}} = V_{	ext{ss}} \)
- 011: \( V_{	ext{ref}} = V_{	ext{REF}}, \) and \( V_{	ext{ref}} = V_{	ext{ss}} \)
- 100: \( V_{	ext{ref}} = V_{	ext{REF}}, \) and \( V_{	ext{ref}} = V_{	ext{REF}} \)
- 101: \( V_{	ext{ref}} = V_{	ext{REF}}, \) and \( V_{	ext{ref}} = V_{	ext{REF}} \)
- 110: \( V_{	ext{ref}} = V_{	ext{REF}}, \) and \( V_{	ext{ref}} = V_{	ext{REF}} \)
- 111: \( V_{	ext{ref}} = V_{	ext{REF}}, \) and \( V_{	ext{ref}} = V_{	ext{REF}} \)

### ADC10SHTx Bits 12-11
- ADC10 sample-and-hold time
  - 00: \( 4 \times \text{ADC10CLKs} \)
  - 01: \( 8 \times \text{ADC10CLKs} \)
  - 10: \( 16 \times \text{ADC10CLKs} \)
  - 11: \( 64 \times \text{ADC10CLKs} \)

### ADC10SR Bit 10
- ADC10 sampling rate. This bit selects the reference buffer drive capability for the maximum sampling rate.
  - 0: Reference buffer supports up to \(-200\) ksp/s
  - 1: Reference buffer supports up to \(-50\) ksp/s

### REFOUT Bit 9
- Reference output
  - 0: Reference output off
  - 1: Reference output on

### REFBURST Bit 8
- Reference burst
  - 0: Reference buffer on continuously
  - 1: Reference buffer on only during sample-and-conversion

### MSC Bit 7
- Multiple sample and conversion. Valid only for sequence or repeated modes.
  - 0: The sampling requires a rising edge of the SH signal to trigger each sample-and-conversion.
  - 1: The first rising edge of the SH signal triggers the sampling time, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed

### REF2_SV Bit 6
- Reference-generator voltage. REFON must also be set.
  - 0: 1.5 V
  - 1: 2.5 V

### REFON Bit 5
- Reference generator on
  - 0: Reference off
  - 1: Reference on

### ADC10ON Bit 4
- ADC10 on
  - 0: ADC10 off
  - 1: ADC10 on

### ADC10IE Bit 3
- ADC10 interrupt enable
  - 0: Interrupt disabled
  - 1: Interrupt enabled

### ADC10IFG Bit 2
- ADC10 interrupt flag. This bit is set if ADC10MEM is loaded with a conversion result. It is automatically reset when the interrupt request is accepted, or it may be reset by software. When using the DTC this flag is set when a block of transfers is completed.
  - 0: No interrupt pending
  - 1: Interrupt pending

### ENC Bit 1
- Enable conversion
  - 0: ADC10 disabled
  - 1: ADC10 enabled

### ADC10SC Bit 0
- Start conversion. Software-controlled sample-and-conversion start. ADC10SC and ENC may be set together with one instruction. ADC10SC is reset automatically.
  - 0: No sample-and-conversion start
  - 1: Start sample-and-conversion
ADC10CTL1 ADC10 Control Register 1

<table>
<thead>
<tr>
<th>INCHx</th>
<th>SHSx</th>
<th>ADC10DF</th>
<th>ISSH</th>
<th>ADC10DIVx</th>
<th>ADC10SSELx</th>
<th>Convex</th>
<th>ADC10BUSY</th>
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Can be modified only when ENC = 0

INCHx Bits 15-12: Input channel select. These bits select the channel for a single-conversion or the highest channel for a sequence of conversions. Only available ADC channels should be selected. See device specific datasheet.

0000 A0
0001 A1
0010 A2
0011 A3
0100 A4
0101 A5
0110 A6
0111 A7
1000 \( V_{\text{REF}} \)
1001 \( V_{\text{REF}}/2 \)
1010 Temperature sensor
1011 \( (V_{\text{REF}} - V_{\text{IN}})/2 \)
1100 \( (V_{\text{REF}} + V_{\text{IN}})/2 \)
1101 \( (V_{\text{REF}} + V_{\text{IN}})/2 \), A12 on MSP430F22x devices
1110 \( (V_{\text{REF}} + V_{\text{IN}})/2 \), A13 on MSP430F22x devices
1111 \( (V_{\text{REF}} + V_{\text{IN}})/2 \), A15 on MSP430F22x devices

SHSx Bits 11-10: Sample-and-hold source select.

00 ADC10DC bit
01 Timer_A.OUT(1)
10 Timer_A.OUT(1)
11 Timer_A.OUT2 (Timer_A.OUT1 on MSP430F20x0, MSP430G2x3, and MSP430G2x30 devices)(1)

ADC10DF Bit 9: ADC10 data format

0 Straight binary
1 2s complement

ISSH Bit 8: Invert signal sample-and-hold

0 The sample-input signal is not inverted.
1 The sample-input signal is inverted.

ADC10DIVx Bits 7-5: ADC10 clock divider

000 /1
001 /2
010 /3
011 /4
100 /5
101 /6
110 /7
111 /8

ADC10SSELx Bits 4-3: ADC10 clock source select

00 ADC10OSC
01 ACLK
10 MCLK
11 SMCLK

CONSEQx Bits 2-1: Conversion sequence mode select

00 Single-channel single-conversion
01 Sequence-of-channels
10 Repeat single-channel
11 Repeat sequence-of-channels

ADC10BUSY Bit 0: ADC10 busy. This bit indicates an active sample or conversion operation

0 No operation is active.
1 A sequence, sample, or conversion is active.
ADC10AE0 Analog (Input) Enable Control Register 0

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ADC10AE0x Bits 7-0 ADC10 analog enable. These bits enable the corresponding pin for analog input. Bit 0 corresponds to A0, Bit 1 corresponds to A1, etc. The analog enable bit of not implemented channels should not be programmed to 1.
- 0 Analog input disabled
- 1 Analog input enabled

ADC10AE1 Analog (Input) Enable Control Register 1

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ADC10AE1x Bits 7-4 ADC10 analog enable. These bits enable the corresponding pin for analog input. Bit 4 corresponds to A12, Bit 5 corresponds to A13, Bit 6 corresponds to A14, and Bit 7 corresponds to A15. The analog enable bit of not implemented channels should not be programmed to 1.
- 0 Analog input disabled
- 1 Analog input enabled

Reserved Bits 3-0 Reserved

ADC10MEM Conversion-Memory Register, Binary Format (Read Only Register)

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<tr>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>Conversion Result</td>
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This is the data format of ADC10MEM when Bit ADC10DF is 0

Conversion Result, Bits 15-0, The 10-bit conversion results are right justified, straight-binary format. Bit 9 is the MSB. Bits 15-10 are always 0.

ADC10MEM Conversion-Memory Register, 2s Complement Format (Read Only Register)

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<td>0</td>
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<td>0</td>
<td>0</td>
<td>Conversion Result</td>
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This is the data format of ADC10MEM when Bit ADC10DF is 1

Conversion Result Bits 15-0, The 10-bit conversion result is left-justified, 2s complement format. Bit 15 is the MSB. Bits 5-0 are always 0.
ADC10DTC0 ADC10 Data Transfer Control Register 0

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Reserved  
Bits 7-4 Reserves. Always read as 0.
ADC10TB  
Bit 3 ADC10 two-block mode
0 One-block transfer mode
1 Two-block transfer mode
ADC10CT  
Bit 2 ADC10 continuous transfer
0 Data transfer stops when one block (one-block mode) or two blocks (two-block mode) have completed.
1 Data is transferred continuously. DTC operation is stopped only if ADC10CT cleared, or ADC10SA is written to.
ADC10B1  
Bit 1 ADC10 block one. This bit indicates for two-block mode which block is filled with ADC10 conversion results. ADC10B1 is valid only after ADC10/FG has been set the first time during DTC operation. ADC10TB must also be set.
0 Block 2 is filled
1 Block 1 is filled
ADC10FETCH  
Bit 0 This bit should normally be reset

ADC10DTC1 ADC10 Data Transfer Control Register 1

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DTC Transfers

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DTC Transfers: Bits 7-0 DTC transfers. These bits define the number of transfers in each block.
0 DTC is disabled
01h-0FFh Number of transfers per block

ADC10SA Start Address Register for Data Transfer

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
|     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

ADC10SAx  
Bits 15-1 ADC10 start address. These bits are the start address for the DTC. A write to register ADC10SA is required to initiate DTC transfers.

Unused  
Bit 0 Unused. Read only. Always read as 0.