1. Solder the RC filter circuit connected to P4.4 needed for exercise 3. See the demo board for help. Use an R value of 10kΩ and a C value of 0.1μF.

2. In your own words, explain the function of the following three lines of code.
   
   // Timer A Config
   TACCTL0 = CCIE;
   TACCR0 = 24000;
   TACTL = TASSEL_2 + MC_1 + ID_2;
   
   Also, what is the resulting timer clock rate (assume SMCLK is running at 16MHz)? This is also the rate at which the Timer A interrupt service routine would be called.

3. Suppose Timer A is sourced from SMCLK running at 16MHz. Write out the contents of the TACCR0 register for generating the following Timer A ISR rates.
   a. 1 kHz
   b. 10 kHz
   
   *Hint for c and d:* To achieve the following two rates you need to modify a second register. What register and what needs to be changed?
   c. Period = 5ms
   d. Period = 25ms

4. Sketch a 10-kHz, 20% duty cycle PWM signal.

5. Assume that TACCTL1 = OUTMOD_7 (reset/set). For each of the configurations in problem 3, write out the contents of the TACCR1 register for generating PWM duty cycles of 15%, 30%, and 65%. Also write the frequency of the PWM signal.

6. What is the single line of code that configures the P1.2 pin to be TA1? In other words, what pin can be either P1.2 or TA1 and what line of code configures it as TA1?

7. Draw the schematic for an RC low pass filter. From the below list of resistors and capacitors, choose values for R and C that results in a cutoff frequency as close as possible to 150Hz. Show your work.
   - Resistors: 220 Ω, 470 Ω, 1 kΩ, 2.2 kΩ, 10 kΩ
   - Capacitors: 0.01 μF, 0.022 μF, 0.1 μF, 1.5 μF

8. Assume you filtered a 10-kHz PWM signal through the circuit you designed above. Write a simple linear equation that relates output voltage to PWM duty cycle (ignoring the slight ripple) and compute the output voltage for duty cycles of 15%, 50%, and 80%. The PWM signal’s low is ground (0V) and its high is 3.3V.