8.1 Digital I/O Introduction

MSP430 devices have up to eight digital I/O ports implemented, P1 to P8. Each port has up to eight I/O pins. Every I/O pin is individually configurable for input or output direction, and each I/O line can be individually read or written to.

Ports P1 and P2 have interrupt capability. Each interrupt for the P1 and P2 I/O lines can be individually enabled and configured to provide an interrupt on a rising edge or falling edge of an input signal. All P1 I/O lines source a single interrupt vector, and all P2 I/O lines source a different, single interrupt vector.

The digital I/O features include:

- Independently programmable individual I/Os
- Any combination of input or output
- Individually configurable P1 and P2 interrupts
- Independent input and output data registers
- Individually configurable pullup or pulldown resistors
- Individually configurable pin-oscillator function (some MSP430 devices)

NOTE: **MSP430G22x0** : These devices feature digital I/O pins P1.2, P1.5, P1.6 and P1.7. The GPIOs P1.0, P1.1, P1.3, P1.4, P2.6, and P2.7 are implemented on this device but not available on the device pin-out. To avoid floating inputs, these GPIOs, these digital I/Os should be properly initialized by running a start-up code. See initialization code below:
mov.b #0x1B, P1REN; ; Terminate unavailable Port1 pins properly ; Config as Input with pull-down enabled
xor.b #0x20, BCSCTL3; ; Select VLO as low freq clock
The initialization code configures GPIOs P1.0, P1.1, P1.3, and P1.4 as inputs with pull-down resistor enabled (that is, P1REN.x = 1) and GPIOs P2.6 and P2.7 are terminated by selecting VLOCLK as ACLK – see the Basic Clock System chapter for details. The register bits of P1.0, P1.1, P1.3, and P1.4 in registers P1OUT, P1DIR, P1IFG, P1IE, P1IES, P1SEL and P1REN should not be altered after the initialization code is executed. Also, all Port2 registers are should not be altered.

8.2 Digital I/O Operation

The digital I/O is configured with user software. The setup and operation of the digital I/O is discussed in the following sections.

8.2.1 Input Register PxIN

Each bit in each PxIN register reflects the value of the input signal at the corresponding I/O pin when the pin is configured as I/O function.

Bit = 0: The input is low

Bit = 1: The input is high

NOTE: **Writing to Read-Only Registers PxIN**

Writing to these read-only registers results in increased current consumption while the write attempt is active.

8.2.2 Output Registers PxOUT

Each bit in each PxOUT register is the value to be output on the corresponding I/O pin when the pin is configured as I/O function, output direction, and the pullup/down resistor is disabled.

Bit = 0: The output is low

Bit = 1: The output is high

If the pin's pullup/pulldown resistor is enabled, the corresponding bit in the PxOUT register selects pullup or pulldown.

Bit = 0: The pin is pulled down

Bit = 1: The pin is pulled up

8.2.3 Direction Registers PxDIR

Each bit in each PxDIR register selects the direction of the corresponding I/O pin, regardless of the selected function for the pin. PxDIR bits for I/O pins that are selected for other functions must be set as required by the other function.

Bit = 0: The port pin is switched to input direction

Bit = 1: The port pin is switched to output direction

8.2.4 Pullup/Pulldown Resistor Enable Registers PxREN

Each bit in each PxREN register enables or disables the pullup/pulldown resistor of the corresponding I/O pin. The corresponding bit in the PxOUT register selects if the pin is pulled up or pulled down.

Bit = 0: Pullup/pulldown resistor disabled

Bit = 1: Pullup/pulldown resistor enabled

8.2.5 Function Select Registers PxSEL and PxSEL2

Port pins are often multiplexed with other peripheral module functions. See the device-specific data sheet to determine pin functions. Each PxSEL and PxSEL2 bit is used to select the pin function - I/O port or peripheral module function.

Table 8-1. PxSEL and PxSEL2

PxSEL2	PxSEL	Pin Function
0	0	I/O function is selected.
0	1	Primary peripheral module function is selected.
1	0	Reserved. See device-specific data sheet.
1	1	Secondary peripheral module function is selected.

Setting PxSELx = 1 does not automatically set the pin direction. Other peripheral module functions may require the PxDIRx bits to be configured according to the direction needed for the module function. See the pin schematics in the device-specific data sheet.

NOTE: Setting PxREN = 1 When PxSEL = 1

On some I/O ports on the MSP430F261x and MSP430F2416/7/8/9, enabling the pullup/pulldown resistor (PxREN = 1) while the module function is selected (PxSEL = 1) does not disable the logic output driver. This combination is not recommended and may result in unwanted current flow through the internal resistor. See the device-specific data sheet pin schematics for more information.

```
;Output ACLK on P2.0 on MSP430F21x1
  BIS.B   #01h,&P2SEL   ; Select ACLK function for pin
  BIS.B   #01h,&P2DIR   ; Set direction to output *Required*
```

NOTE: P1 and P2 Interrupts Are Disabled When PxSEL = 1

When any P1SELx or P2SELx bit is set, the corresponding pin's interrupt function is disabled. Therefore, signals on these pins will not generate P1 or P2 interrupts, regardless of the state of the corresponding P1IE or P2IE bit.

When a port pin is selected as an input to a peripheral, the input signal to the peripheral is a latched representation of the signal at the device pin. While PxSELx = 1, the internal input signal follows the signal at the pin. However, if the PxSELx = 0, the input to the peripheral maintains the value of the input signal at the device pin before the PxSELx bit was reset.

8.2.6 Pin Oscillator

Some MSP430 devices have a pin oscillator function built-in to some pins. The pin oscillator function may be used in capacitive touch sensing applications to eliminate external passive components. Additionally, the pin oscillator may be used in sensor applications.

No external components to create the oscillation

Capacitive sensors can be connected directly to MSP430 pin

Robust, typical built-in hysteresis of ~0.7 V

When the pin oscillator function is enabled, other pin configurations are overwritten. The output driver is turned off while the weak pullup/pulldown is enabled and controlled by the voltage level on the pin itself. The voltage on the I/O is fed into the Schmitt trigger of the pin and then routed to a timer. The connection to the timer is device specific and, thus, defined in the device-specific data sheet. The Schmitt-trigger output is inverted and then decides if the pullup or the pulldown is enabled. Due to the inversion, the pin starts to oscillate as soon as the pin oscillator pin configuration is selected. Some of the pin-oscillator outputs are combined by a logical OR before routing to a timer clock input or timer capture channel. Therefore, only one pin oscillator should be enabled at a time. The oscillation frequency of each pin is defined by the load on the pin and by the I/O type. I/Os with analog functions typically show a lower oscillation frequency than pure digital I/Os. See the device-specific data sheet for details. Pins without external load show typical oscillation frequencies of 1 MHz to 3 MHz.

Pin oscillator in a cap touch application

A typical touch pad application using the pin oscilator is shown in Figure 8-1.

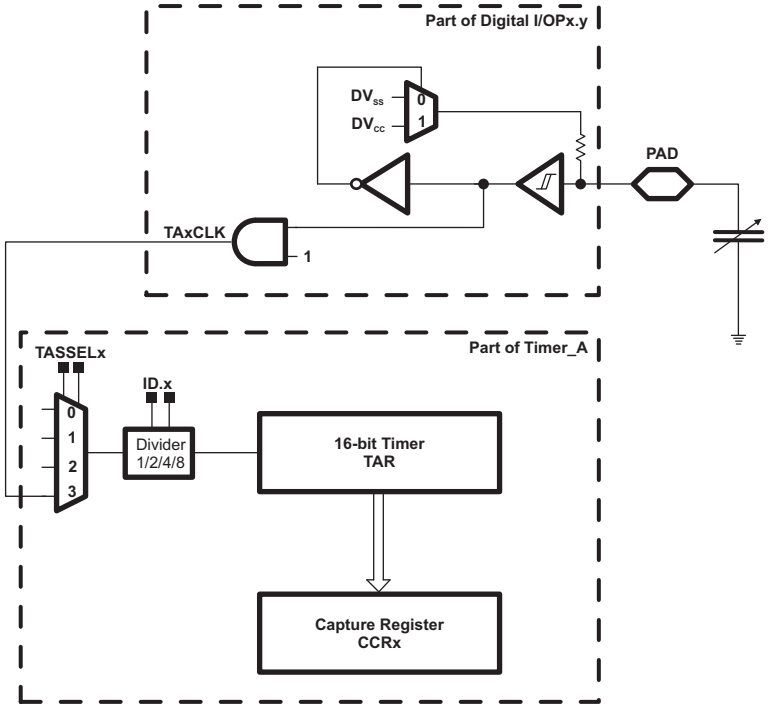


Figure 8-1. Example Circuitry and Configuration using the Pin Oscillator

A change of the capacitance of the touch pad (external capacitive load) has an effect on the pin oscillator frequency. An approaching finger tip increases the capacitance of the touch pad thus leads to a lower self-oscillation frequency due to the longer charging time. The oscillation frequency can directly be captured in a built-in Timer channel. The typical sensitivity of a pin is shown in Figure 8-2.

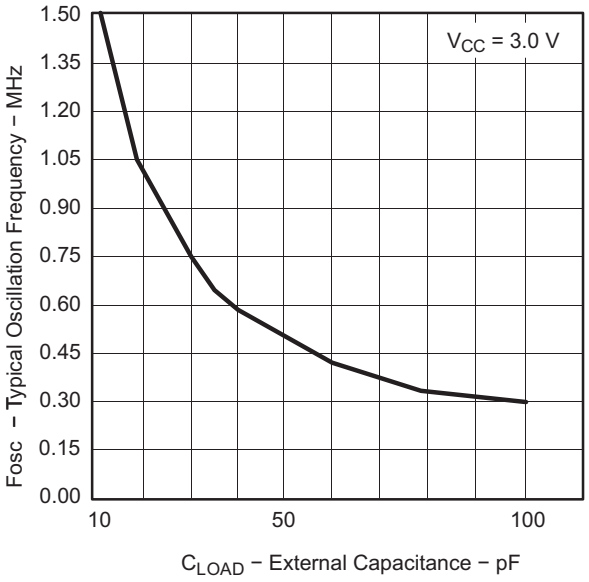


Figure 8-2. Typical Pin-Oscillation Frequency

8.2.7 P1 and P2 Interrupts

Each pin in ports P1 and P2 have interrupt capability, configured with the PxIFG, PxIE, and PxIES registers. All P1 pins source a single interrupt vector, and all P2 pins source a different single interrupt vector. The PxIFG register can be tested to determine the source of a P1 or P2 interrupt.

8.2.7.1 Interrupt Flag Registers P1IFG, P2IFG

Each PxIFGx bit is the interrupt flag for its corresponding I/O pin and is set when the selected input signal edge occurs at the pin. All PxIFGx interrupt flags request an interrupt when their corresponding PxIE bit and the GIE bit are set. Each PxIFG flag must be reset with software. Software can also set each PxIFG flag, providing a way to generate a software initiated interrupt.

Bit = 0: No interrupt is pending

Bit = 1: An interrupt is pending

Only transitions, not static levels, cause interrupts. If any PxIFGx flag becomes set during a Px interrupt service routine, or is set after the RETI instruction of a Px interrupt service routine is executed, the set PxIFGx flag generates another interrupt. This ensures that each transition is acknowledged.

NOTE: PxIFG Flags When Changing PxOUT or PxDIR

Writing to P1OUT, P1DIR, P2OUT, or P2DIR can result in setting the corresponding P1IFG or P2IFG flags.

8.2.7.2 Interrupt Edge Select Registers P1IES, P2IES

Each PxIES bit selects the interrupt edge for the corresponding I/O pin.

Bit = 0: The PxIFGx flag is set with a low-to-high transition

Bit = 1: The PxIFGx flag is set with a high-to-low transition

NOTE: Writing to PxIESx

Writing to P1IES, or P2IES can result in setting the corresponding interrupt flags.

PxIESx	PxINx	PxIFGx
0 → 1	0	May be set
0 → 1	1	Unchanged
1 → 0	0	Unchanged
1 → 0	1	May be set

8.2.7.3 Interrupt Enable P1IE, P2IE

Each PxIE bit enables the associated PxIFG interrupt flag.

Bit = 0: The interrupt is disabled.

Bit = 1: The interrupt is enabled.

8.2.8 Configuring Unused Port Pins

Unused I/O pins should be configured as I/O function, output direction, and left unconnected on the PC board, to prevent a floating input and reduce power consumption. The value of the PxOUT bit is irrelevant, since the pin is unconnected. Alternatively, the integrated pullup/pulldown resistor can be enabled by setting the PxREN bit of the unused pin to prevent the floating input. See the *System Resets, Interrupts, and Operating Modes* chapter for termination of unused pins.

8.3 Digital I/O Registers

The digital I/O registers are listed in Table 8-2.

Table 8-2. Digital I/O Registers

Port	Register	Short Form	Address	Register Type	Initial State
P1	Input	P1IN	020h	Read only	-
	Output	P1OUT	021h	Read/write	Unchanged
	Direction	P1DIR	022h	Read/write	Reset with PUC
	Interrupt Flag	P1IFG	023h	Read/write	Reset with PUC
	Interrupt Edge Select	P1IES	024h	Read/write	Unchanged
	Interrupt Enable	P1IE	025h	Read/write	Reset with PUC
	Port Select	P1SEL	026h	Read/write	Reset with PUC
	Port Select 2	P1SEL2	041h	Read/write	Reset with PUC
	Resistor Enable	P1REN	027h	Read/write	Reset with PUC
P2	Input	P2IN	028h	Read only	-
	Output	P2OUT	029h	Read/write	Unchanged
	Direction	P2DIR	02Ah	Read/write	Reset with PUC
	Interrupt Flag	P2IFG	02Bh	Read/write	Reset with PUC
	Interrupt Edge Select	P2IES	02Ch	Read/write	Unchanged
	Interrupt Enable	P2IE	02Dh	Read/write	Reset with PUC
	Port Select	P2SEL	02Eh	Read/write	0C0h with PUC
	Port Select 2	P2SEL2	042h	Read/write	Reset with PUC
	Resistor Enable	P2REN	02Fh	Read/write	Reset with PUC
P3	Input	P3IN	018h	Read only	-
	Output	P3OUT	019h	Read/write	Unchanged
	Direction	P3DIR	01Ah	Read/write	Reset with PUC
	Port Select	P3SEL	01Bh	Read/write	Reset with PUC
	Port Select 2	P3SEL2	043h	Read/write	Reset with PUC
	Resistor Enable	P3REN	010h	Read/write	Reset with PUC
P4	Input	P4IN	01Ch	Read only	-
	Output	P4OUT	01Dh	Read/write	Unchanged
	Direction	P4DIR	01Eh	Read/write	Reset with PUC
	Port Select	P4SEL	01Fh	Read/write	Reset with PUC
	Port Select 2	P4SEL2	044h	Read/write	Reset with PUC
	Resistor Enable	P4REN	011h	Read/write	Reset with PUC
P5	Input	P5IN	030h	Read only	-
	Output	P5OUT	031h	Read/write	Unchanged
	Direction	P5DIR	032h	Read/write	Reset with PUC
	Port Select	P5SEL	033h	Read/write	Reset with PUC
	Port Select 2	P5SEL2	045h	Read/write	Reset with PUC
	Resistor Enable	P5REN	012h	Read/write	Reset with PUC
P6	Input	P6IN	034h	Read only	-
	Output	P6OUT	035h	Read/write	Unchanged
	Direction	P6DIR	036h	Read/write	Reset with PUC
	Port Select	P6SEL	037h	Read/write	Reset with PUC
	Port Select 2	P6SEL2	046h	Read/write	Reset with PUC
	Resistor Enable	P6REN	013h	Read/write	Reset with PUC

8.2.1 Input Register PxIN

Each bit in each PxIN register reflects the value of the input signal at the corresponding I/O pin when the pin is configured as I/O function.

7	6	5	4	3	2	1	0
PxIN.7	**PxIN.6**	**PxIN.5**	**PxIN.4**	**PxIN.3**	**PxIN.2**	**PxIN.1**	**PxIN.0**
R	r	r	r	r	r	r	r

PxIN.0	Bit 0	0	IF PxDIR.0 = 0 PxIN.0 pin is LOW
		1	IF PxDIR.0 = 0 PxIN.0 pin is HIGH
PxIN.1	Bit 1	0	IF PxDIR.1 = 0 PxIN.1 pin is LOW
		1	IF PxDIR.1 = 0 PxIN.1 pin is HIGH
PxIN.2	Bit 2	0	IF PxDIR.2 = 0 PxIN.2 pin is LOW
		1	IF PxDIR.2 = 0 PxIN.2 pin is HIGH
PxIN.3	Bit 3	0	IF PxDIR.3 = 0 PxIN.3 pin is LOW
		1	IF PxDIR.3 = 0 PxIN.3 pin is HIGH
PxIN.4	Bit 4	0	IF PxDIR.4 = 0 PxIN.4 pin is LOW
		1	IF PxDIR.4 = 0 PxIN.4 pin is HIGH
PxIN.5	Bit 5	0	IF PxDIR.5 = 0 PxIN.5 pin is LOW
		1	IF PxDIR.5 = 0 PxIN.5 pin is HIGH
PxIN.6	Bit 6	0	IF PxDIR.6 = 0 PxIN.6 pin is LOW
		1	IF PxDIR.6 = 0 PxIN.6 pin is HIGH
PxIN.7	Bit 7	0	IF PxDIR.7 = 0 PxIN.7 pin is LOW
		1	IF PxDIR.7 = 0 PxIN.7 pin is HIGH

NOTE: Writing to Read-Only Registers PxIN

Writing to these read-only registers results in increased current consumption while the write attempt is active.

8.2.2 Output Registers PxOUT

7	6	5	4	3	2	1	0
PxOUT.7	PxOUT.6	PxOUT.5	PxOUT.4	PxOUT.3	PxOUT.2	PxOUT.1	PxOUT.0
rw (x)	rw (x)	rw (x)	rw (x)	rw (x)	rw (x)	rw (x)	rw (x)

PxOUT.0	Bit 0	If Pin0 configured as I/O function, output direction and its resistor is disabled: 0 Pin0 output Low 1 Pin0 output High If Pin0 configured as I/O function and its resistor is enabled: 0 Pin0 is pulled down 1 Pin0 is pulled up
PxOUT.1	Bit 1	If Pin1 configured as I/O function, output direction and its resistor is disabled: 0 Pin1 output Low 1 Pin1 output High If Pin1 configured as I/O function and its resistor is enabled: 0 Pin1 is pulled down 1 Pin1 is pulled up
PxOUT.2	Bit 2	If Pin2 configured as I/O function, output direction and its resistor is disabled: 0 Pin2 output Low 1 Pin2 output High If Pin2 configured as I/O function and its resistor is enabled: 0 Pin2 is pulled down 1 Pin2 is pulled up
PxOUT.3	Bit 3	If Pin3 configured as I/O function, output direction and its resistor is disabled: 0 Pin3 output Low 1 Pin3 output High If Pin3 configured as I/O function and its resistor is enabled: 0 Pin3 is pulled down 1 Pin3 is pulled up
PxOUT.4	Bit 4	If Pin4 configured as I/O function, output direction and its resistor is disabled: 0 Pin4 output Low 1 Pin4 output High If Pin4 configured as I/O function and its resistor is enabled: 0 Pin4 is pulled down 1 Pin4 is pulled up
PxOUT.5	Bit 5	If Pin5 configured as I/O function, output direction and its resistor is disabled: 0 Pin5 output Low 1 Pin5 output High If Pin5 configured as I/O function and its resistor is enabled: 0 Pin5 is pulled down 1 Pin5 is pulled up
PxOUT.6	Bit 6	If Pin6 configured as I/O function, output direction and its resistor is disabled: 0 Pin6 output Low 1 Pin6 output High If Pin6 configured as I/O function and its resistor is enabled: 0 Pin6 is pulled down 1 Pin6 is pulled up
PxOUT.7	Bit 7	If Pin7 configured as I/O function, output direction and its resistor is disabled: 0 Pin7 output Low 1 Pin7 output High If Pin7 configured as I/O function and its resistor is enabled: 0 Pin7 is pulled down 1 Pin7 is pulled up

8.2.3 Direction Registers PxDIR

Each bit in each PxDIR register selects the direction of the corresponding I/O pin, regardless of the selected function for the pin. PxDIR bits for I/O pins that are selected for other functions must be set as required by the other function

.

7	6	5	4	3	2	1	0
PxDIR.7	PxDIR.6	PxDIR.5	PxDIR.4	PxDIR.3	PxDIR.2	PxDIR.1	PxDIR.0
rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)

PxDIR.0	Bit 0	0 1	Port Pin0 is switched to input direction Port Pin0 is switched to output direction
PxDIR.1	Bit 1	0 1	Port Pin1 is switched to input direction Port Pin1 is switched to output direction
PxDIR.2	Bit 2	0 1	Port Pin2 is switched to input direction Port Pin2 is switched to output direction
PxDIR.3	Bit 3	0 1	Port Pin3 is switched to input direction Port Pin3 is switched to output direction
PxDIR.4	Bit 4	0 1	Port Pin4 is switched to input direction Port Pin4 is switched to output direction
PxDIR.5	Bit 5	0 1	Port Pin5 is switched to input direction Port Pin5 is switched to output direction
PxDIR.6	Bit 6	0 1	Port Pin6 is switched to input direction Port Pin6 is switched to output direction
PxDIR.7	Bit 7	0 1	Port Pin7 is switched to input direction Port Pin7 is switched to output direction

8.2.4 Pullup/Pulldown Resistor Enable Registers PxREN

Each bit in each PxREN register enables or disables the pullup/pulldown resistor of the corresponding I/O pin. **The corresponding bit in the PxOUT register selects if the pin is pulled up or pulled down.**

7	6	5	4	3	2	1	0
PxREN.7	PxREN.6	PxREN.5	PxREN.4	PxREN.3	PxREN.2	PxREN.1	PxREN.0
rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)

PxREN.0	Bit 0	0 1	Port Pin0's Resistor Disabled/Not Connected Port Pin0's Resistor Enabled, *PxOUT.0 determines if it is used as Pullup or Pulldown resistor.*
PxREN.1	Bit 1	0 1	Port Pin1's Resistor Disabled/Not Connected Port Pin1's Resistor Enabled, *PxOUT.1 determines if it is used as Pullup or Pulldown resistor.*
PxREN.2	Bit 2	0 1	Port Pin2's Resistor Disabled/Not Connected Port Pin2's Resistor Enabled, *PxOUT.2 determines if it is used as Pullup or Pulldown resistor.*
PxREN.3	Bit 3	0 1	Port Pin3's Resistor Disabled/Not Connected Port Pin3's Resistor Enabled, *PxOUT.3 determines if it is used as Pullup or Pulldown resistor.*
PxREN.4	Bit 4	0 1	Port Pin4's Resistor Disabled/Not Connected Port Pin4's Resistor Enabled, *PxOUT.4 determines if it is used as Pullup or Pulldown resistor.*
PxREN.5	Bit 5	0 1	Port Pin5's Resistor Disabled/Not Connected Port Pin5's Resistor Enabled, *PxOUT.5 determines if it is used as Pullup or Pulldown resistor.*
PxREN.6	Bit 6	0 1	Port Pin6's Resistor Disabled/Not Connected Port Pin6's Resistor Enabled, *PxOUT.6 determines if it is used as Pullup or Pulldown resistor.*
PxREN.7	Bit 7	0 1	Port Pin7's Resistor Disabled/Not Connected Port Pin7's Resistor Enabled, *PxOUT.7 determines if it is used as Pullup or Pulldown resistor.*

8.2.5 Function Select Registers PxSEL

Port pins are often multiplexed with other peripheral module functions. See the device-specific data sheet to determine pin functions. Each PxSEL bit is used to select the pin function - I/O port or peripheral module function.

7	6	5	4	3	2	1	0
PxSEL.7	**PxSEL.6**	**PxSEL.5**	**PxSEL.4**	**PxSEL.3**	**PxSEL.2**	**PxSEL.1**	**PxSEL.0**
rw (0) *(P2SEL rw(1))*	rw (0) (*P2SEL rw(1)*)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)

PxSEL.0	Bit 0	0 1	Select I/O function, pin is Px.0 Peripheral module function selected (See DataSheet)
PxSEL.1	Bit 1	0 1	Select I/O function, pin is Px.1 Peripheral module function selected (See DataSheet)
PxSEL.2	Bit 2	0 1	Select I/O function, pin is Px.2 Peripheral module function selected (See DataSheet)
PxSEL.3	Bit 3	0 1	Select I/O function, pin is Px.3 Peripheral module function selected (See DataSheet)
PxSEL.4	Bit 4	0 1	Select I/O function, pin is Px.4 Peripheral module function selected (See DataSheet)
PxSEL.5	Bit 5	0 1	Select I/O function, pin is Px.5 Peripheral module function selected (See DataSheet)
PxSEL.6	Bit 6	0 1	Select I/O function, pin is Px.6 Peripheral module function selected (See DataSheet)
PxSEL.7	Bit 7	0 1	Select I/O function, pin is Px.7 Peripheral module function selected (See DataSheet)

Setting PxSEL = 1 does not automatically set the pin direction. Other peripheral module functions may require the PxDIR bits to be configured according to the direction needed for the module function. See the pin schematics in the device-specific data sheet.

8.2.7 P1 and P2 Interrupts

Each pin in ports P1 and P2 have interrupt capability, configured with the PxIFG, PxIE, and PxIES registers. All P1 pins source a single interrupt vector, and all P2 pins source a different single interrupt vector. The PxIFG register can be tested to determine the source of a P1 or P2 interrupt.

8.2.7.1 Interrupt Flag Registers P1IFG, P2IFG

Each PxIFGx bit is the interrupt flag for its corresponding I/O pin and is set when the selected input signal edge occurs at the pin. All PxIFGx interrupt flags request an interrupt when their corresponding PxIE bit and the GIE bit are set. Each PxIFG flag must be reset with software. Software can also set each PxIFG flag, providing a way to generate a software initiated interrupt.

7	6	5	4	3	2	1	0
PxIFG.7	PxIFG.6	PxIFG.5	PxIFG.4	PxIFG.3	PxIFG.2	PxIFG.1	PxIFG.0
rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)

PxIFG.0	Bit 0	0 1	Port Pin0, No interrupt is pending Port Pin0, An interrupt is pending
PxIFG.1	Bit 1	0 1	Port Pin1, No interrupt is pending Port Pin1, An interrupt is pending
PxIFG.2	Bit 2	0 1	Port Pin2, No interrupt is pending Port Pin2, An interrupt is pending
PxIFG.3	Bit 3	0 1	Port Pin3, No interrupt is pending Port Pin3, An interrupt is pending
PxIFG.4	Bit 4	0 1	Port Pin4, No interrupt is pending Port Pin4, An interrupt is pending
PxIFG.5	Bit 5	0 1	Port Pin5, No interrupt is pending Port Pin5, An interrupt is pending
PxIFG.6	Bit 6	0 1	Port Pin6, No interrupt is pending Port Pin6, An interrupt is pending
PxIFG.7	Bit 7	0 1	Port Pin7, No interrupt is pending Port Pin7, An interrupt is pending

Only transitions, not static levels, cause interrupts. If any PxIFGx flag becomes set during a Px interrupt service routine, or is set after the RETI instruction of a Px interrupt service routine is executed, the set PxIFGx flag generates another interrupt. This ensures that each transition is acknowledged.

NOTE: PxIFG Flags When Changing PxOUT or PxDIR

Writing to P1OUT, P1DIR, P2OUT, or P2DIR can result in setting the corresponding P1IFG or P2IFG flags.

8.2.7.2 Interrupt Edge Select Registers P1IES, P2IES

Each PxIES bit selects the interrupt edge for the corresponding I/O pin.

7	6	5	4	3	2	1	0
PxIES.7	PxIES.6	PxIES.5	PxIES.4	PxIES.3	PxIES.2	PxIES1	PxIES.0
rw (x)	rw (x)	rw (x)	rw (x)	rw (x)	rw (x)	rw (x)	rw (x)

PxIES.0	Bit 0	0 1	Pin0, PxIFG.0 flag is set with a low-to-high transition Pin0, PxIFG.0 flag is set with a high-to-low transition
PxIES.1	Bit 1	0 1	Pin1, PxIFG.1 flag is set with a low-to-high transition Pin1, PxIFG.1 flag is set with a high-to-low transition
PxIES.2	Bit 2	0 1	Pin2, PxIFG.2 flag is set with a low-to-high transition Pin2, PxIFG.2 flag is set with a high-to-low transition
PxIES.3	Bit 3	0 1	Pin3, PxIFG.3 flag is set with a low-to-high transition Pin3, PxIFG.3 flag is set with a high-to-low transition
PxIES.4	Bit 4	0 1	Pin4, PxIFG.4 flag is set with a low-to-high transition Pin4, PxIFG.4 flag is set with a high-to-low transition
PxIES.5	Bit 5	0 1	Pin5, PxIFG.5 flag is set with a low-to-high transition Pin5, PxIFG.5 flag is set with a high-to-low transition
PxIES.6	Bit 6	0 1	Pin6, PxIFG.6 flag is set with a low-to-high transition Pin6, PxIFG.6 flag is set with a high-to-low transition
PxIES.7	Bit 7	0 1	Pin7, PxIFG.7 flag is set with a low-to-high transition Pin7, PxIFG.7 flag is set with a high-to-low transition

8.2.7.3 Interrupt Enable P1IE, P2IE

Each PxIE bit enables the associated PxIFG interrupt flag

7	6	5	4	3	2	1	0
PxIE.7	PxIE.6	PxIE.5	PxIE.4	PxIE.3	PxIE.2	PxIE.1	PxIE.0
rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)	rw (0)

.

PxIE.0	Bit 0	0 1	PxIE.0 interrupt is disabled PxIE.0 interrupt is enabled
PxIE.1	Bit 1	0 1	PxIE.1 interrupt is disabled PxIE.1 interrupt is enabled
PxIE.2	Bit 2	0 1	PxIE.2 interrupt is disabled PxIE.2 interrupt is enabled
PxIE.3	Bit 3	0 1	PxIE.3 interrupt is disabled PxIE.3 interrupt is enabled
PxIE.4	Bit 4	0 1	PxIE.4 interrupt is disabled PxIE.4 interrupt is enabled
PxIE.5	Bit 5	0 1	PxIE.5 interrupt is disabled PxIE.5 interrupt is enabled
PxIE.6	Bit 6	0 1	PxIE.6 interrupt is disabled PxIE.6 interrupt is enabled
PxIE.7	Bit 7	0 1	PxIE.7 interrupt is disabled PxIE.7 interrupt is enabled

APPLICATION INFORMATION

Port P1 Pin Schematic: P1.0 to P1.3, Input/Output With Schmitt Trigger

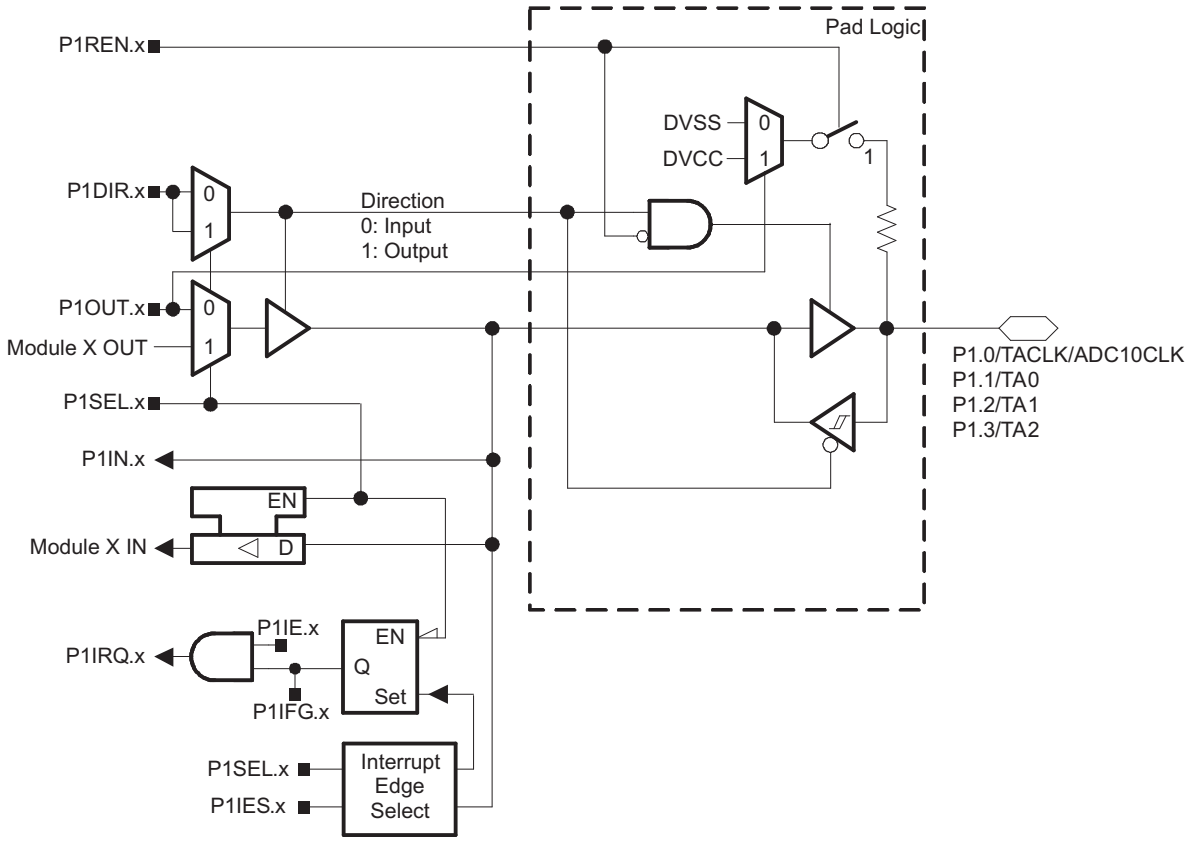


Table 21. Port P1 (P1.0 to P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK/ADC10CLK	0	P1.0 (1)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		ADC10CLK	1	1
P1.1/TA0	1	P1.1 (1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2 (1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TA2	3	P1.3 (1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1

(1) Default after reset (PUC/POR)

Port P1 Pin Schematic: P1.4 to P1.6, Input/Output With Schmitt Trigger and In-System Access Features

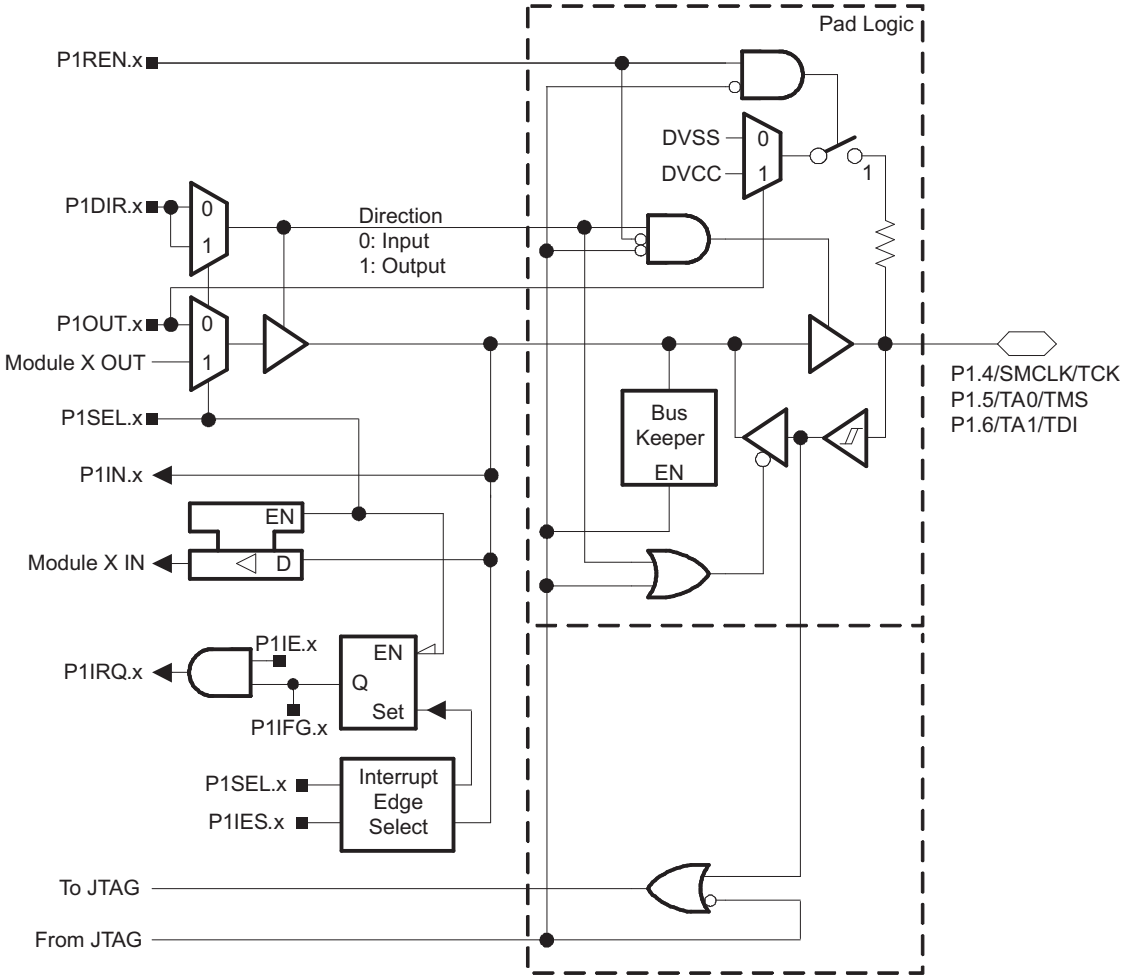


Table 22. Port P1 (P1.4 to P1.6) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.4/SMCLK/TCK	4	P1.4[2] (I/O)	I: 0; O: 1	0	0
		SMCLK	1	1	0
		TCK	X	X	1
P1.5/TA0/TMS	5	P1.5[2] (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA0	1	1	0
		TMS	X	X	1
P1.6/TA1/TDI/TCLK	6	P1.6[2] (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA1	1	1	0
		TDI/TCLK[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Function controlled by JTAG

Port P1 Pin Schematic: P1.7, Input/Output With Schmitt Trigger and In-System Access Features

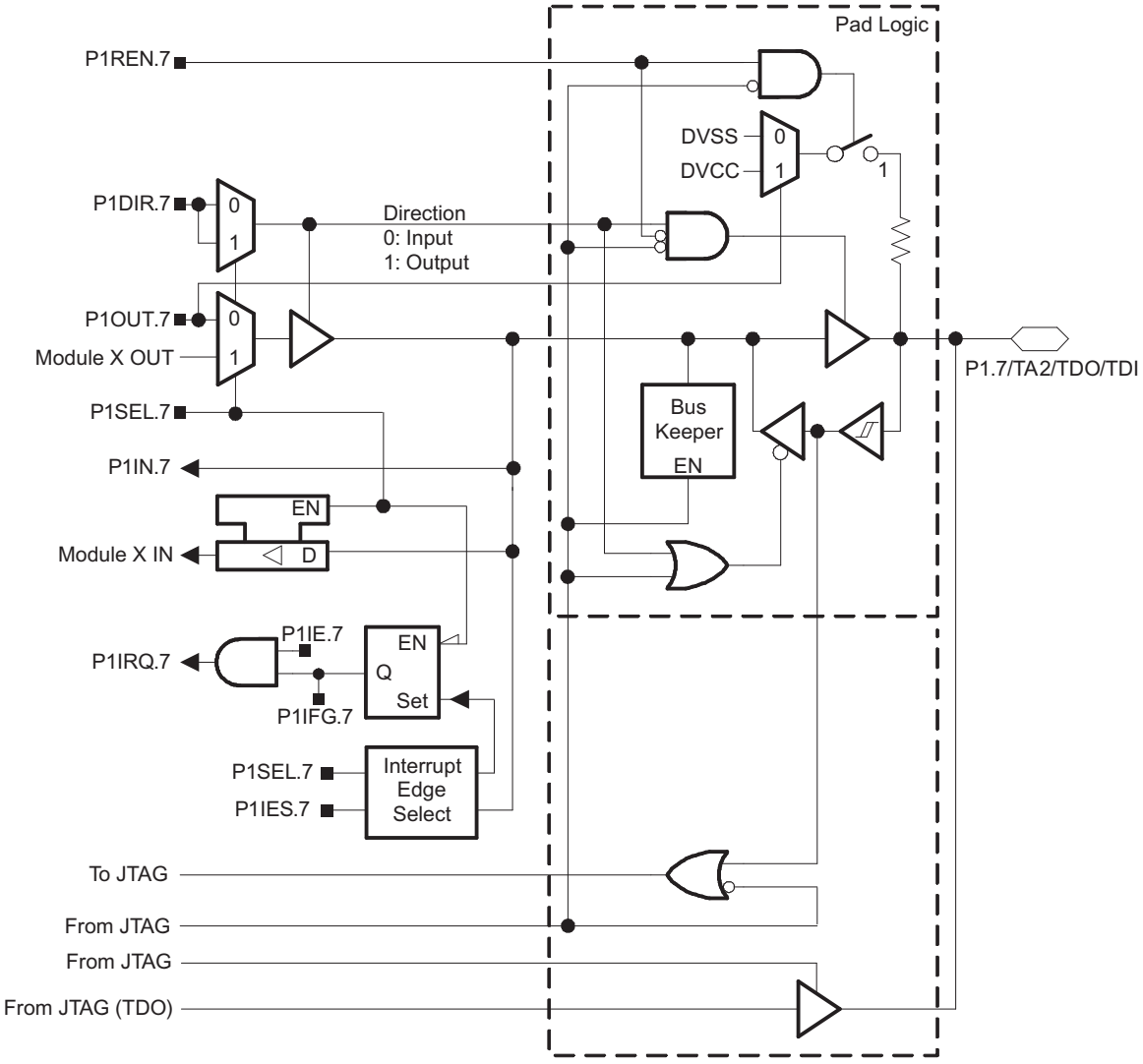


Table 23. Port P1 (P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.7/TA2/TDO/TDI	7	P1.7[2] (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA2	1	1	0
		TDO/TDI[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Function controlled by JTAG

Port P2 Pin Schematic: P2.0, P2.2, Input/Output With Schmitt Trigger

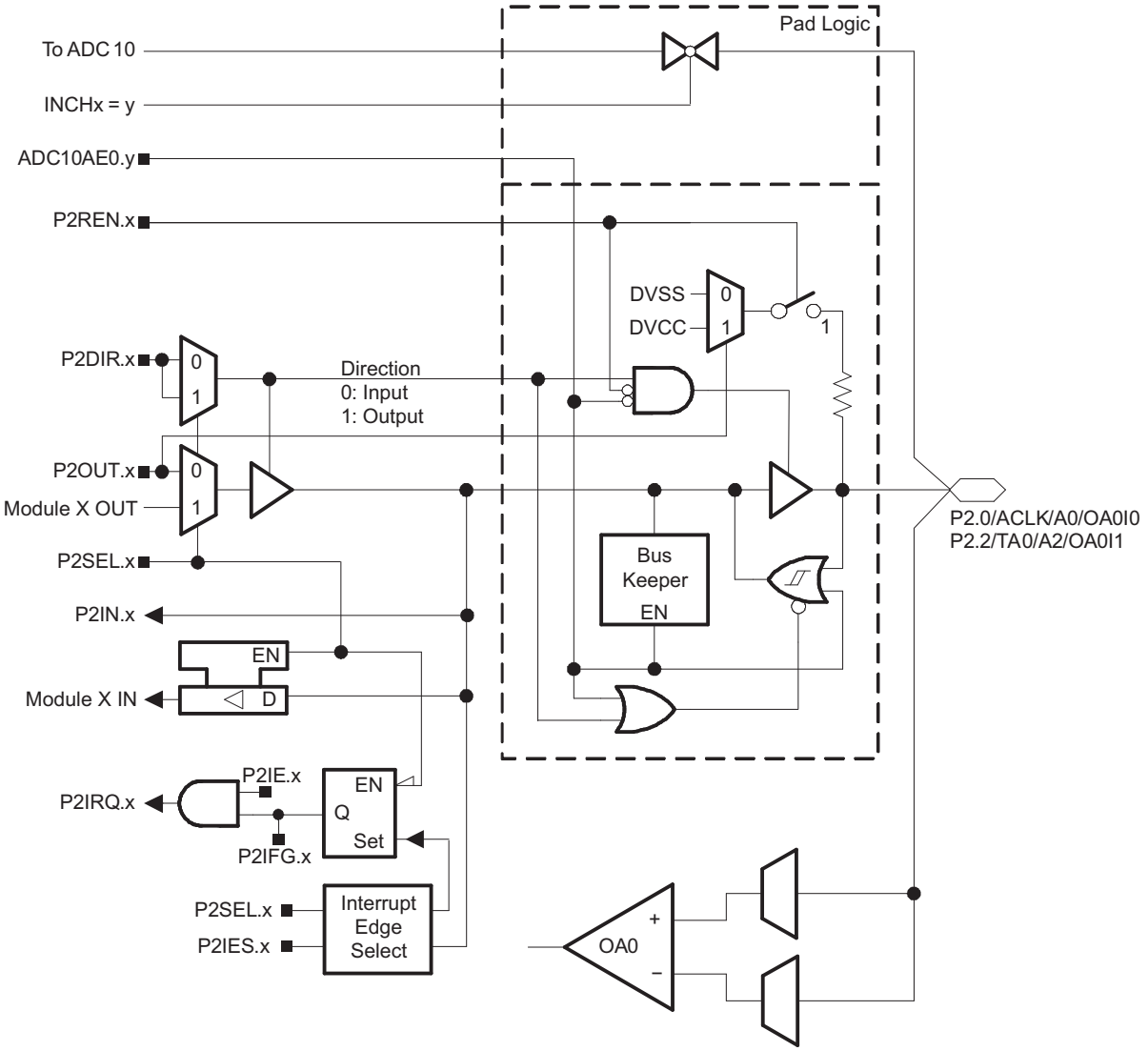


Table 24. Port P2 (P2.0, P2.2) Pin Functions

Pin Name (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS[1]		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.0/ACLK/A0/OA0I0	0	0	P2.0[2] (I/O)	I: 0; O: 1	0	0
			ACLK	1	1	0
			A0/OA0I0[3]	X	X	1
P2.2/TA0/A2/OA0I1	2	2	P2.2[2] (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI0B	0	1	0
			Timer_A3.TA0	1	1	0
			A2/OA0I1[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 Pin Schematic: P2.1, Input/Output With Schmitt Trigger

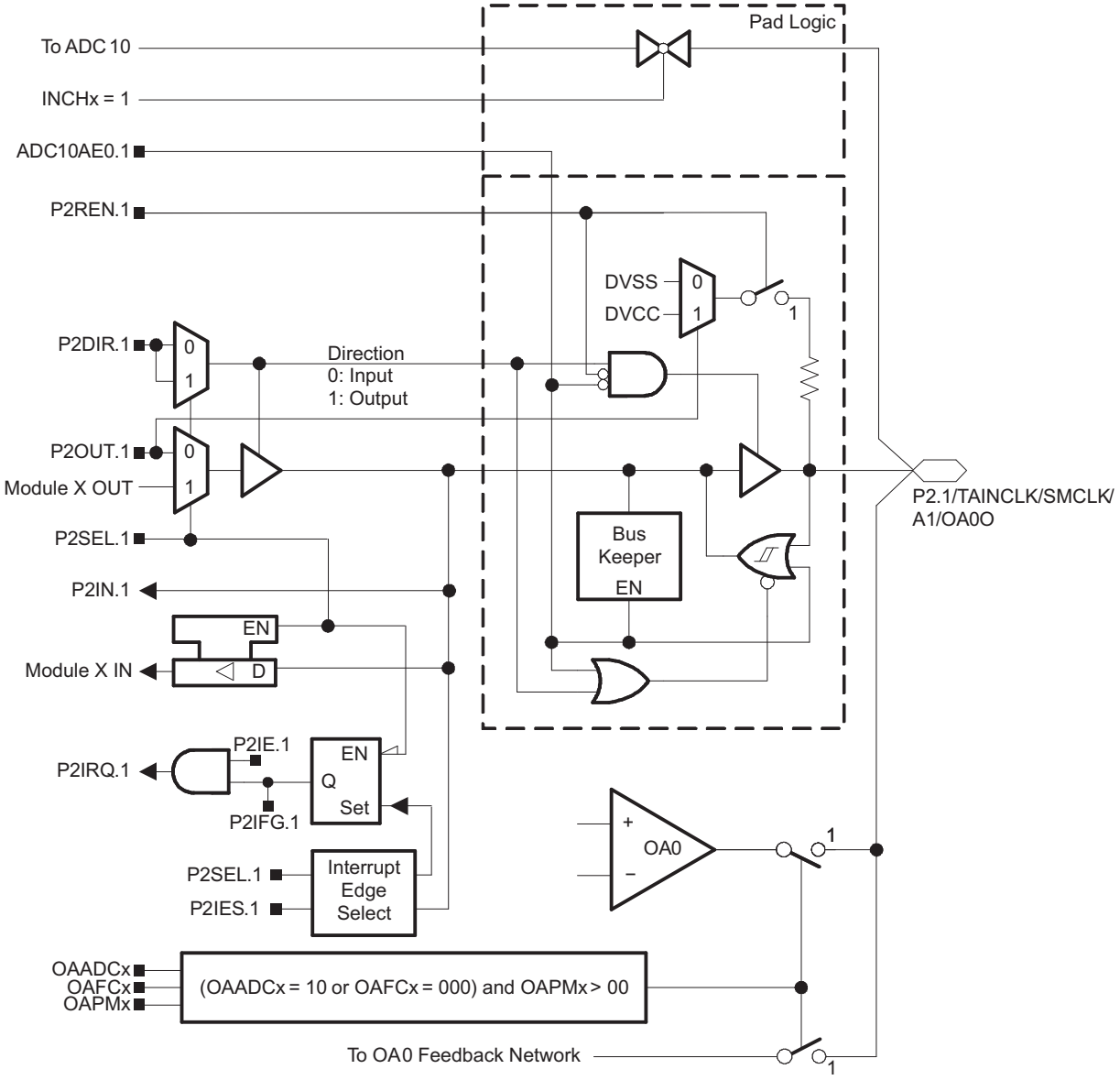


Table 25. Port P2 (P2.1) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS[1]		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.1/TAINCLK/SMCLK/ A1/OA0O	1	1	P2.1[2] (I/O)	I: 0; O: 1	0	0
			Timer_A3.INCLK	0	1	0
			SMCLK	1	1	0
			A1/OA0O[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 Pin Schematic: P2.3, Input/Output With Schmitt Trigger

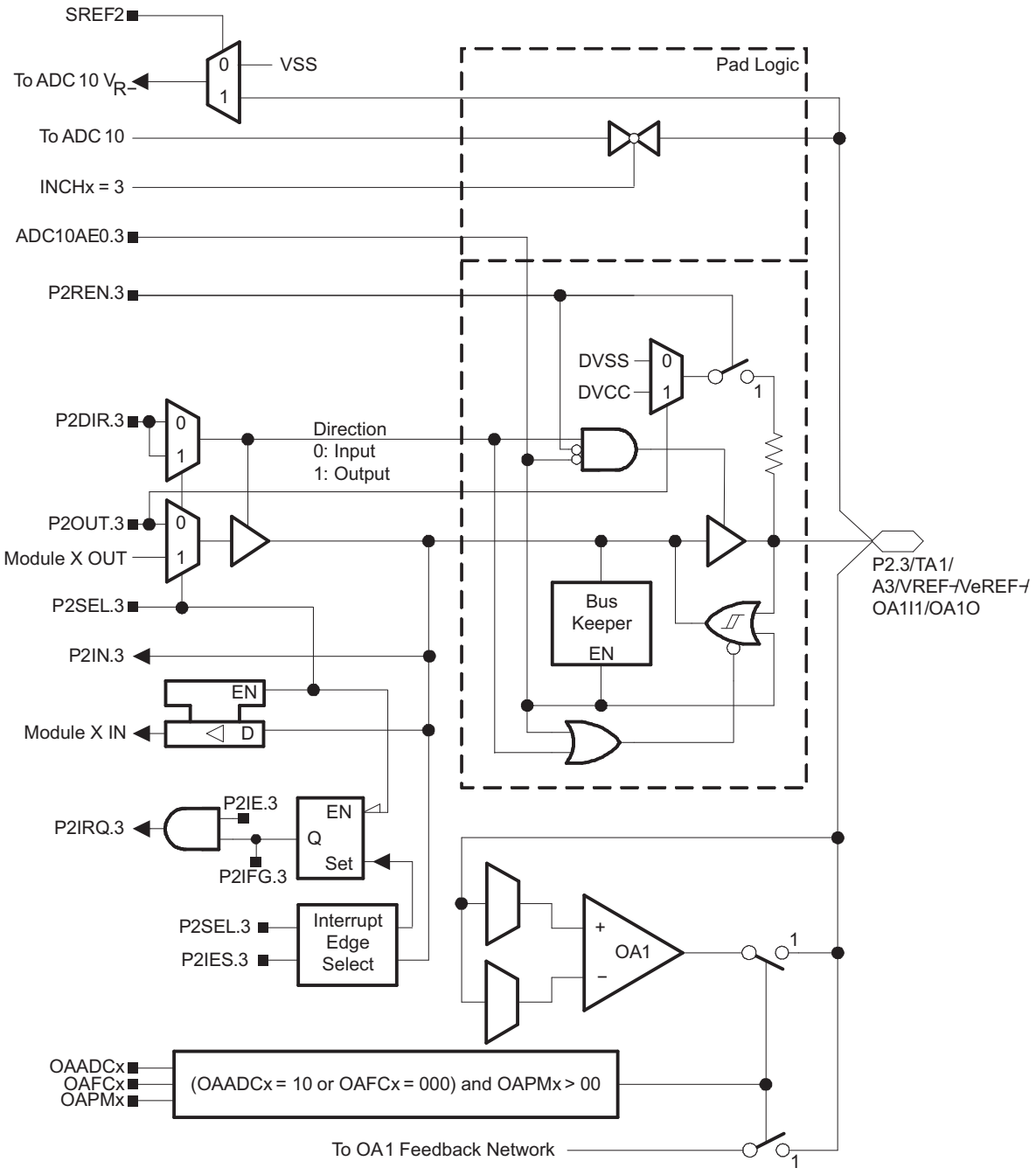


Table 26. Port P2 (P2.3) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS(1)		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.3/TA1/A3/V_{REF-} /V_{eREF-}/ OA1I1/OA1O	3	3	P2.3(2) (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI1B	0	1	0
			Timer_A3.TA1	1	1	0
			A3/V_{REF-}/V_{eREF-}/OA1I1/OA1O(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 Pin Schematic: P2.4, Input/Output With Schmitt Trigger

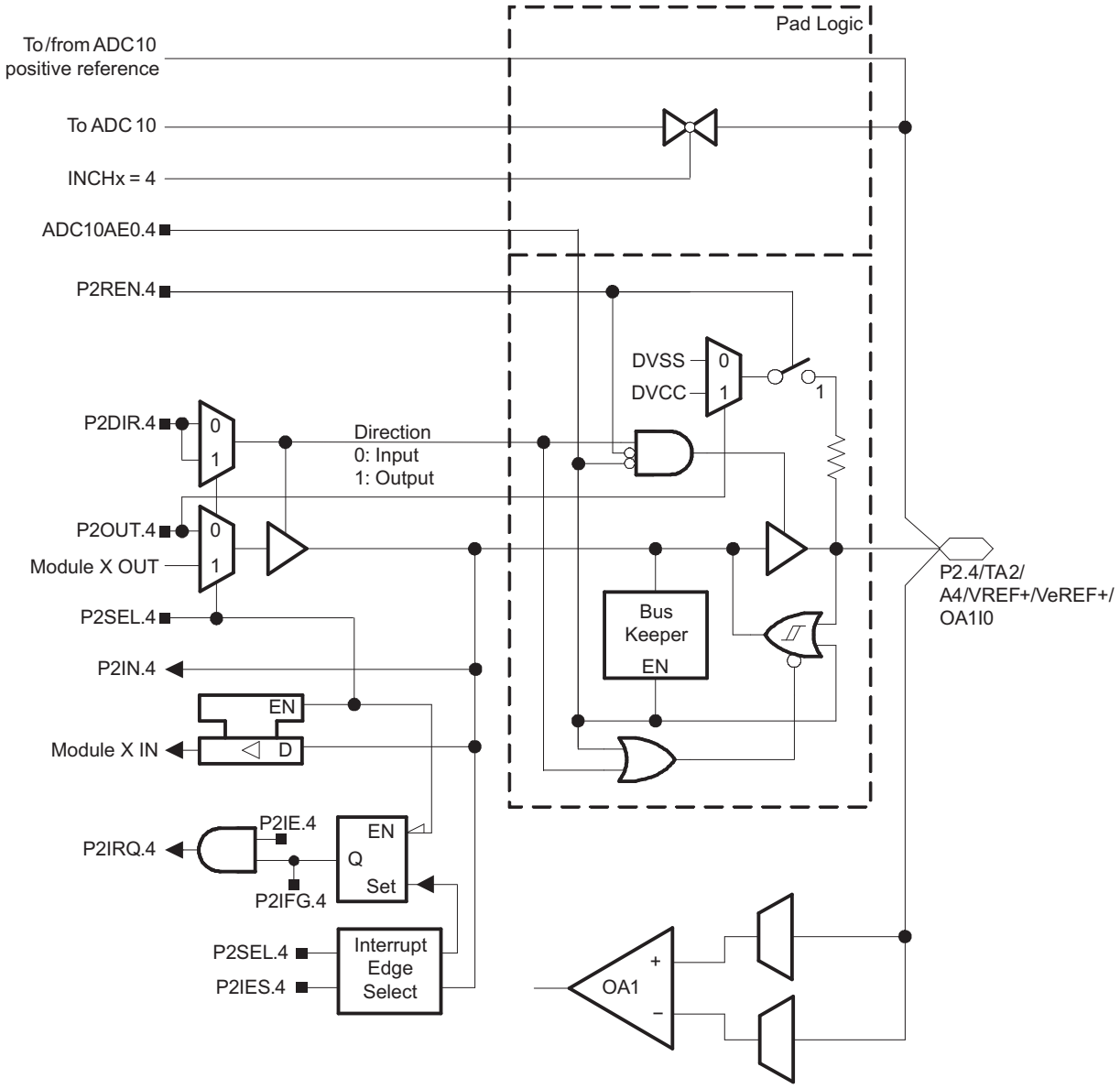


Table 27. Port P2 (P2.4) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS(1)		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.4/TA2/A4/V_{REF+}/ V_{eREF+}/ OA1I0	4	4	P2.4(2) (I/O)	I: 0; O: 1	0	0
			Timer_A3.TA2	1	1	0
			A4/V_{REF+}/V_{eREF+}/OA1I0(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 Pin Schematic: P2.5, Input/Output With Schmitt Trigger and External R_{OSC} for DCO

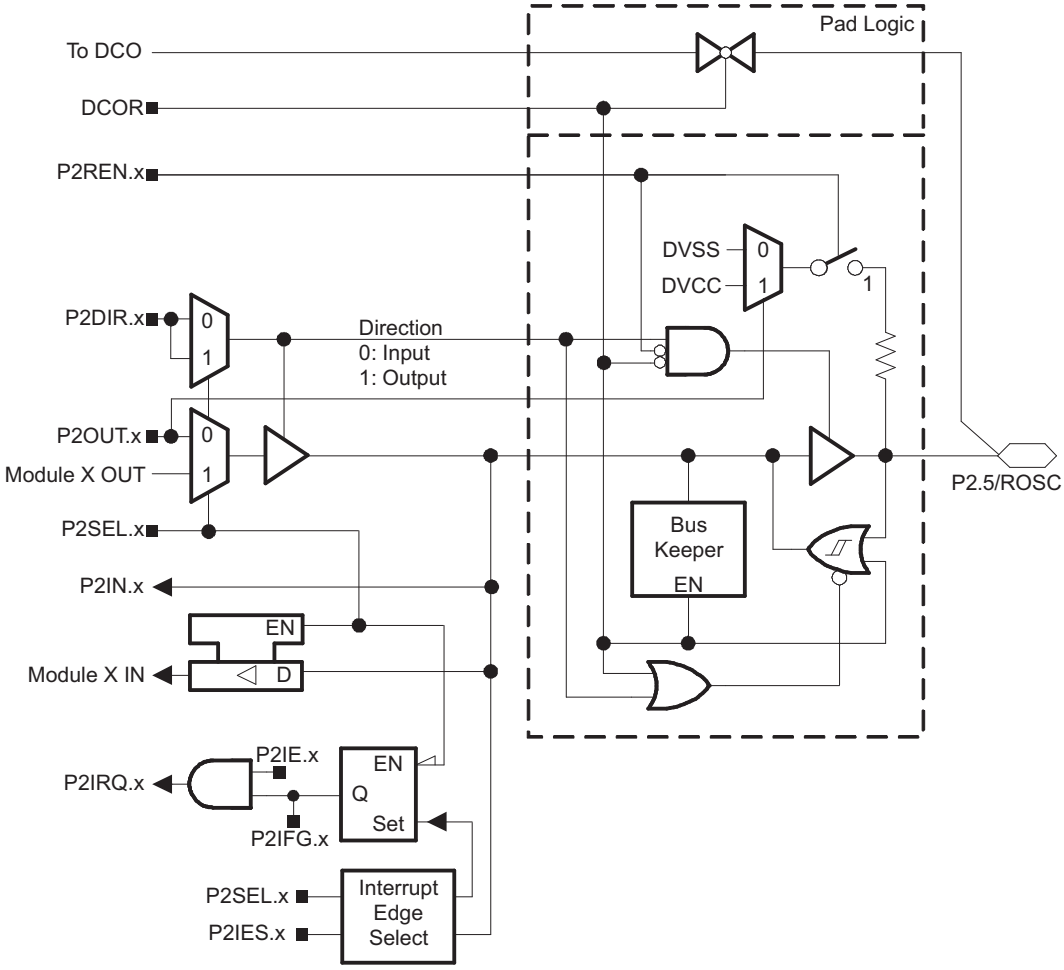


Table 28. Port P2 (P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P2DIR.x	P2SEL.x	DCOR
P2.5/R_{OSC}	5	P2.5[2] (I/O)	I: 0; O: 1	0	0
		N/A[3]	0	1	0
		DV_{SS}	1	1	0
		R_{OSC}	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) N/A = Not available or not applicable

Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger and Crystal Oscillator Input

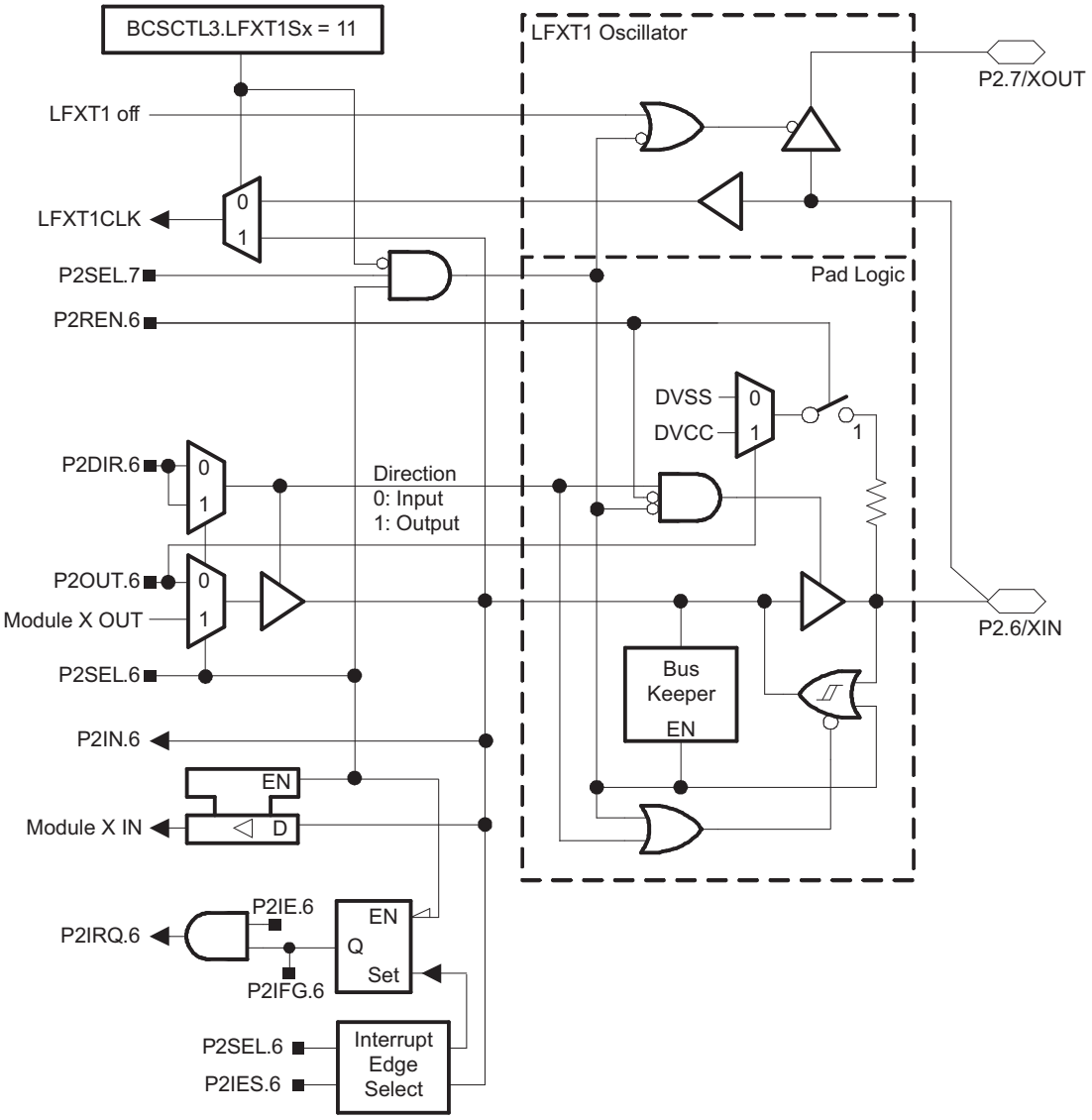


Table 29. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)	
			P2DIR.x	P2SEL.x
P2.6/XIN	6	P2.6 (I/O)	I: 0; O: 1	0
		XIN(2)	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)

Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger and Crystal Oscillator Output

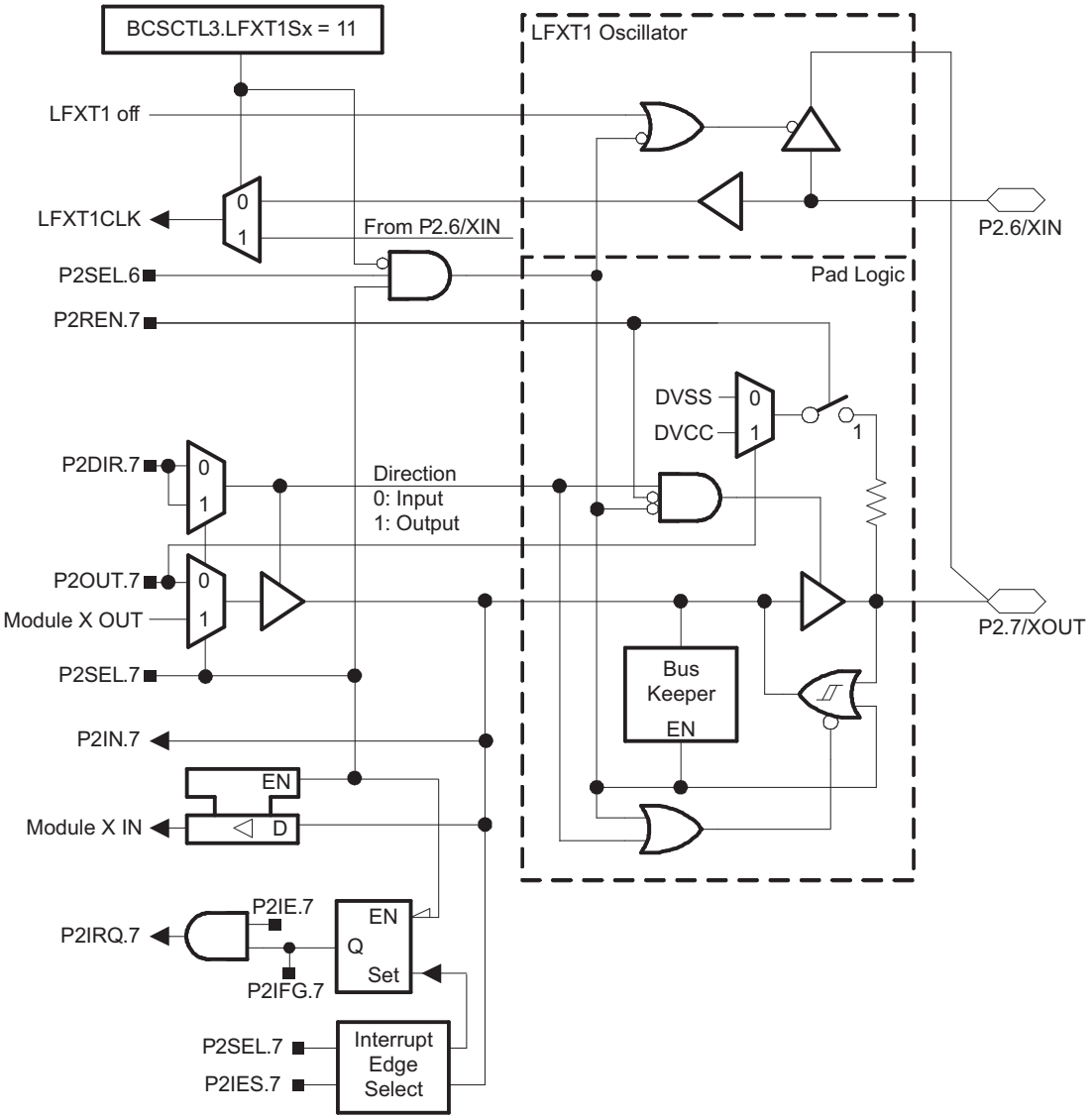


Table 30. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)	
			P2DIR.x	P2SEL.x
XOUT/P2.7	7	P2.7 (I/O)	I: 0; O: 1	0
		XOUT(2) (3)	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) If the pin XOUT/P2.7 is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

Port P3 Pin Schematic: P3.0, Input/Output With Schmitt Trigger

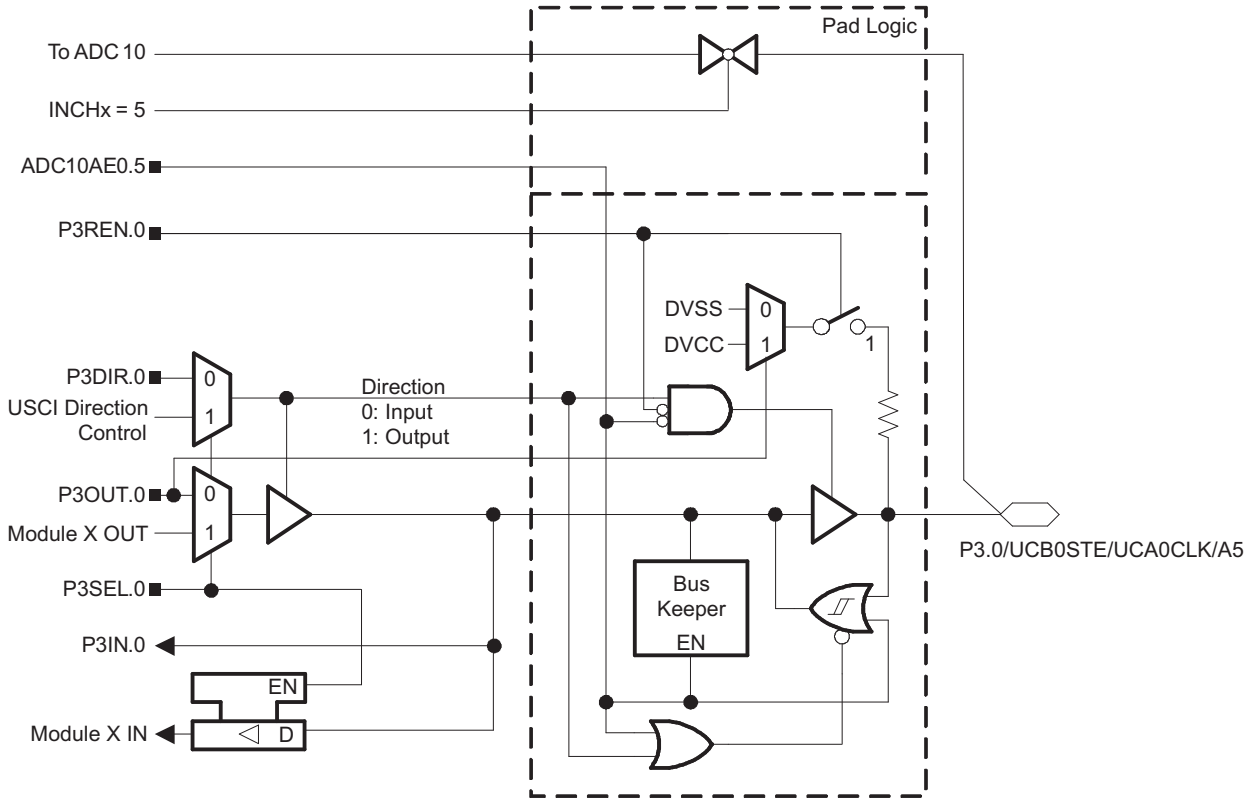


Table 31. Port P3 (P3.0) Pin Functions

PIN NAME (P1.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS(1)		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.0/UCB0STE/ UCA0CLK/A5	0	5	P3.0(2) (I/O)	I: 0; O: 1	0	0
			UCB0STE/UCA0CLK(3) (4)	X	1	0
			A5(5)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) The pin direction is controlled by the USCI module.
(4) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(5) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P3 Pin Schematic: P3.1 to P3.5, Input/Output With Schmitt Trigger

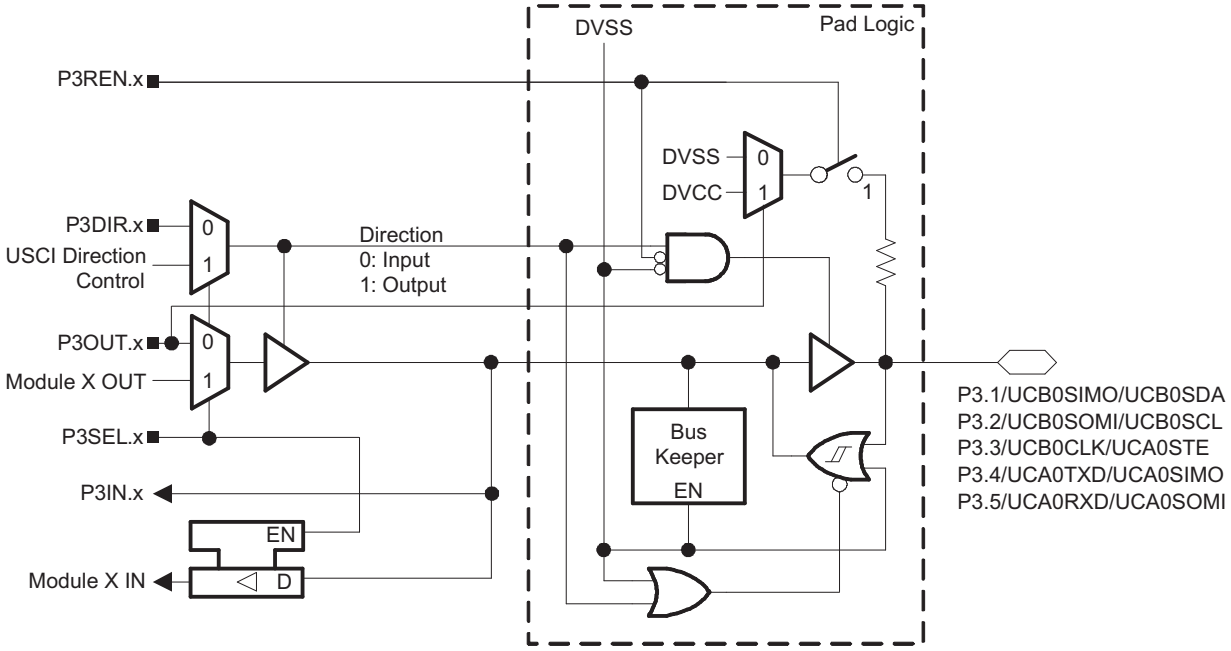


Table 32. Port P3 (P3.1 to P3.5) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)	
			P3DIR.x	P3SEL.x
P3.1/UCB0SIMO/UCB0SDA	1	P3.1(2) (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA(3)	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2(2) (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL(3)	X	1
P3.3/UCB0CLK/UCA0STE	3	P3.3(2) (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE(3) (4)	X	1
P3.4/UCA0TXD/UCA0SIMO	4	P3.4(2) (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO(3)	X	1
P3.5/UCA0RXD/UCA0SOMI	5	P3.5(2) (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI(3)	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) The pin direction is controlled by the USCI module.
(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode even if 4-wire SPI mode is selected.

Port P3 Pin Schematic: P3.6 to P3.7, Input/Output With Schmitt Trigger

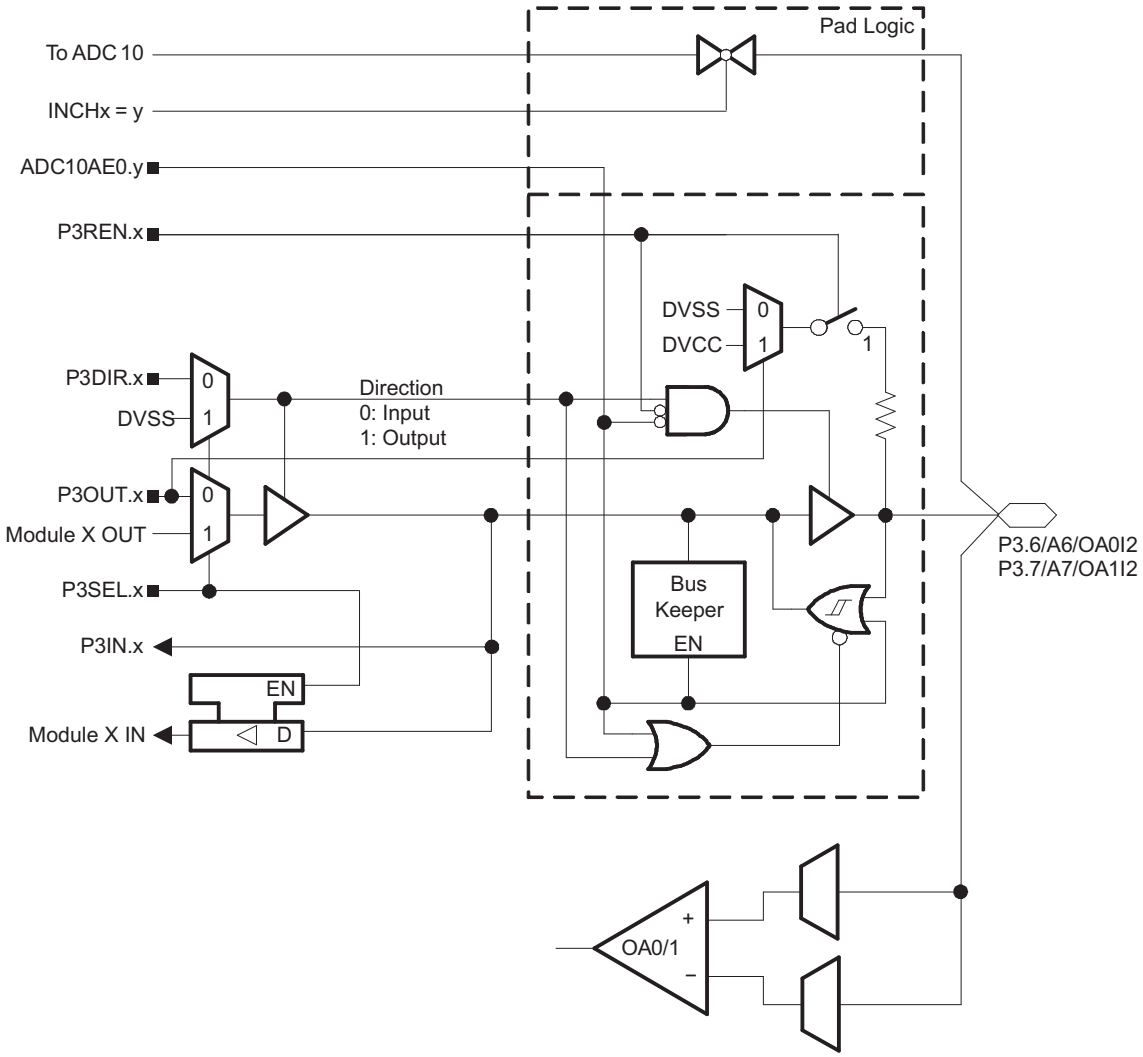


Table 33. Port P3 (P3.6, P3.7) Pin Functions

PIN NAME (P3.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS[1]		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.6/A6/OA0I2	6	6	P3.6[2] (I/O)	I: 0; O: 1	0	0
			A6/OA0I2[3]	X	X	1
P3.7/A7/OA1I2	7	7	P3.7[2] (I/O)	I: 0; O: 1	0	0
			A7/OA1I2[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.0 to P4.2, Input/Output With Schmitt Trigger

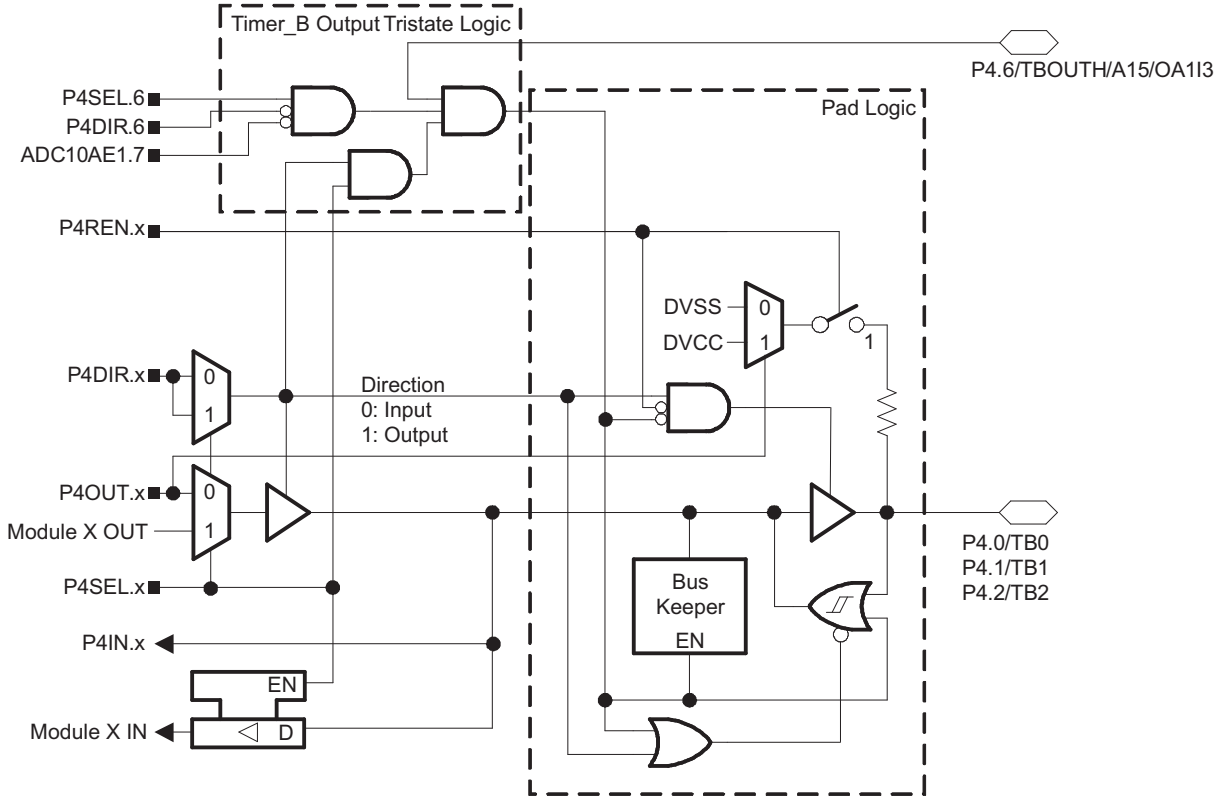
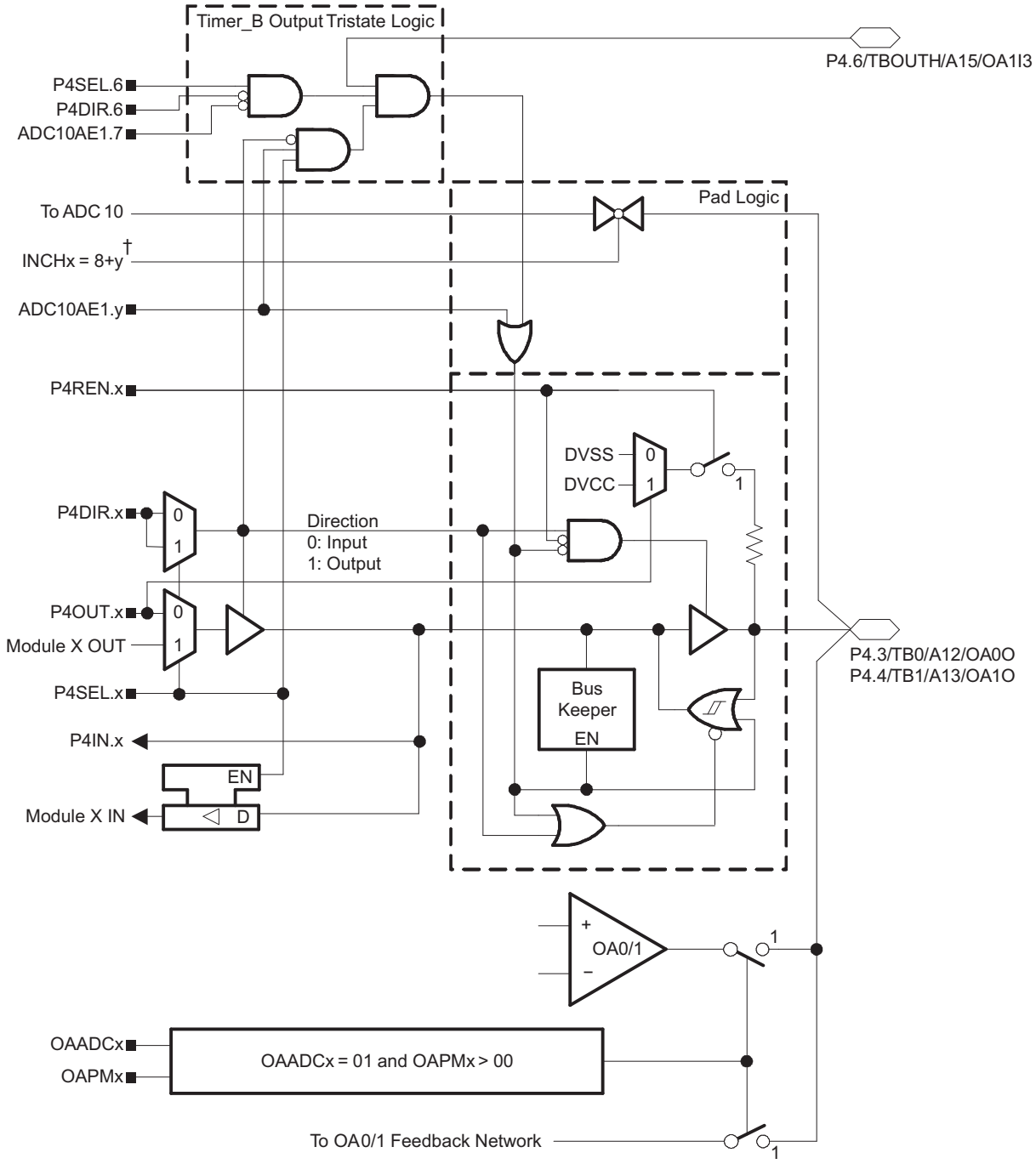


Table 34. Port P4 (P4.0 to P4.2) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0(1) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI0A	0	1
		Timer_B3.TB0	1	1
P4.1/TB1	1	P4.1(1) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.TB1	1	1
P4.2/TB2	2	P4.2(1) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI2A	0	1
		Timer_B3.TB2	1	1

(1) Default after reset (PUC/POR)

Port P4 Pin Schematic: P4.3 to P4.4, Input/Output With Schmitt Trigger



†If OAADCx = 11 and not OAFCx = 000, the ADC input A12 or A13 is internally connected to the OA0 or OA1 output, respectively, and the connections from the ADC and the operational amplifiers to the pad are disabled.

Table 35. Port P4 (P4.3 to P4.4) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS(1)		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.3/TB0/A12/OA0O	3	4	P4.3(2) (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI0B	0	1	0
			Timer_B3.TB0	1	1	0
			A12/OA0O(3)	X	X	1
P4.4/TB1/A13/OA1O	4	5	P4.4(2) (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI1B	0	1	0
			Timer_B3.TB1	1	1	0
			A13/OA1O(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.5, Input/Output With Schmitt Trigger

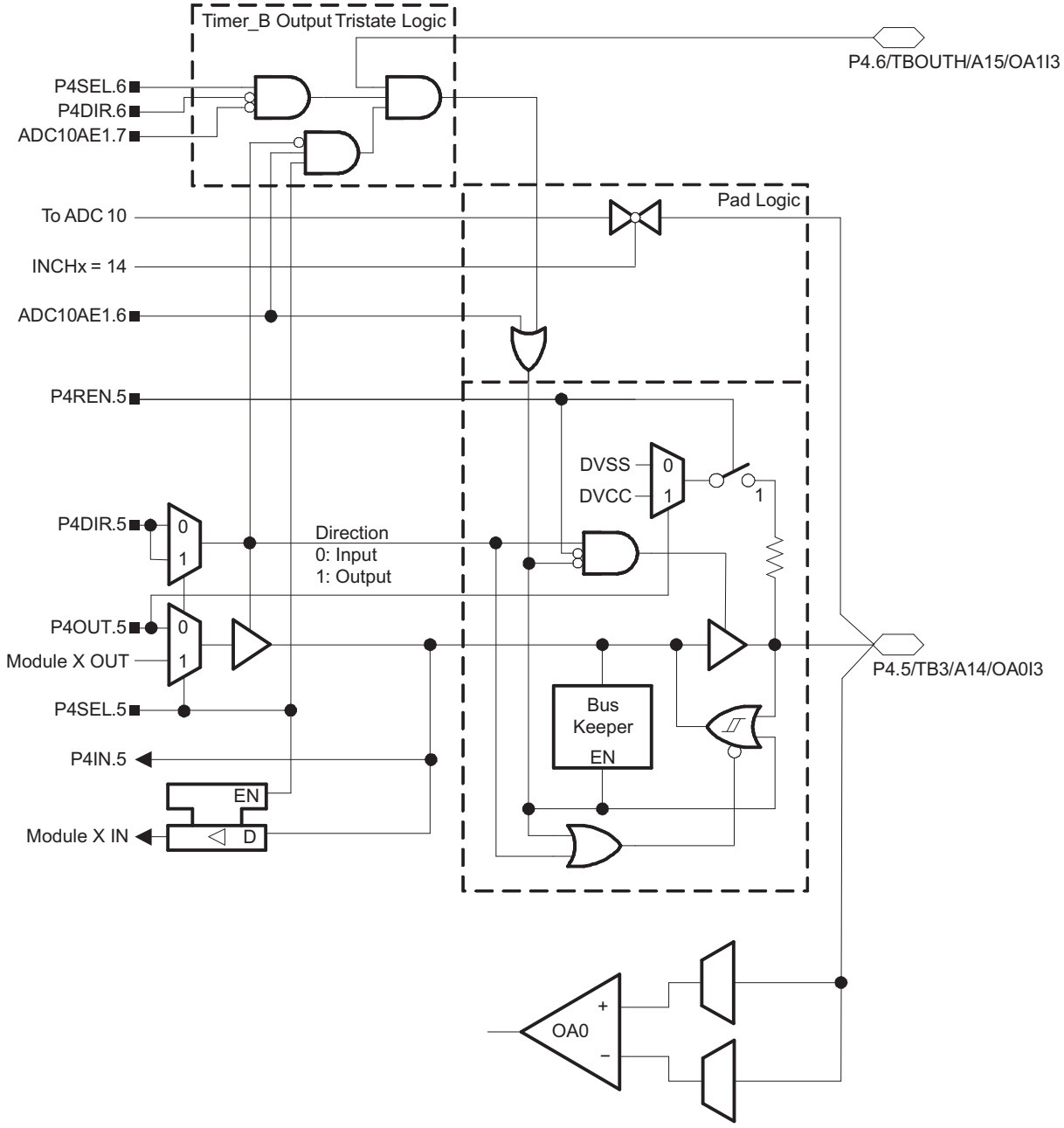


Table 36. Port P4 (P4.5) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS[1]		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.5/TB3/A14/OA0I3	5	6	P4.5[2] (I/O)	I: 0; O: 1	0	0
			Timer_B3.TB2	1	1	0
			A14/OA0I3[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.6, Input/Output With Schmitt Trigger

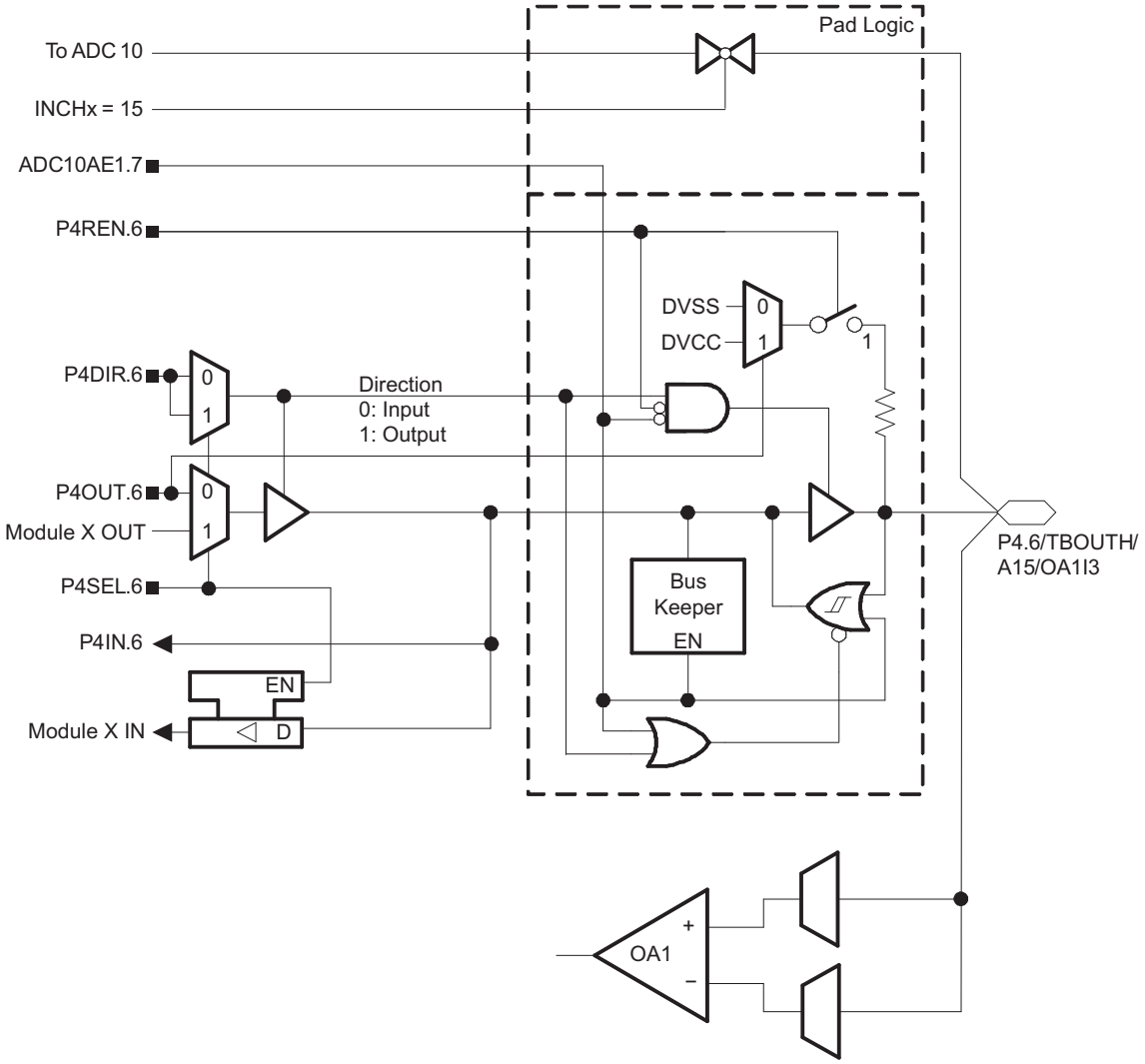


Table 37. Port P4 (P4.6) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS[1]		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.6/TBOUTH/A15/OA1I3	6	7	P4.6[2] (I/O)	I: 0; O: 1	0	0
			TBOUTH	0	1	0
			DV_{SS}	1	1	0
			A15/OA1I3[3]	X	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)
(3) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.7, Input/Output With Schmitt Trigger

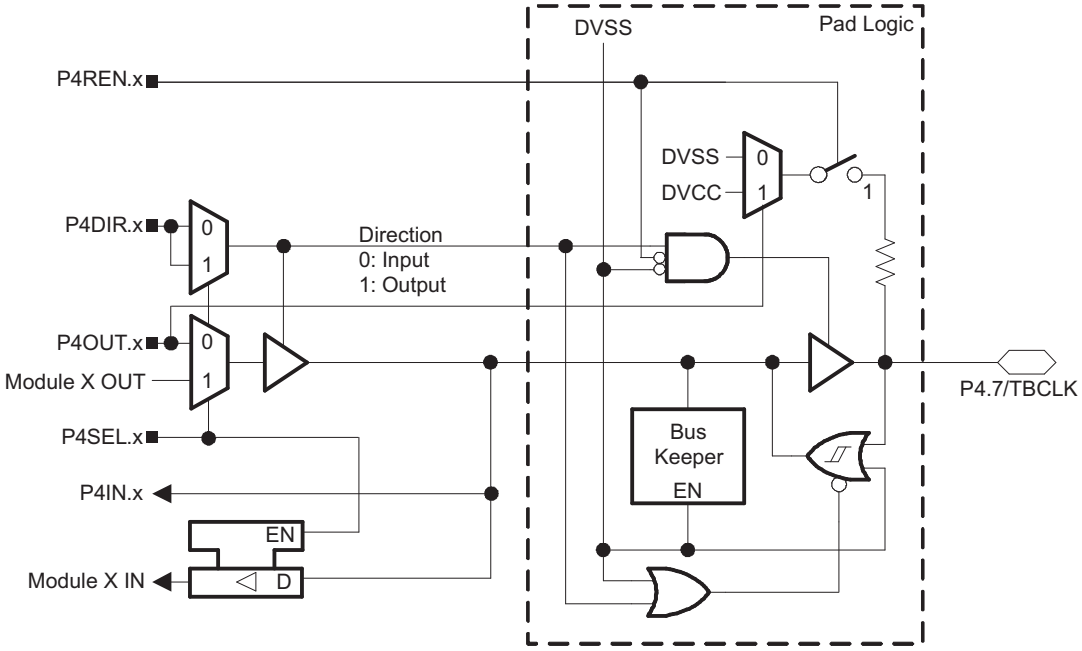


Table 38. Port P4 (Pr.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.7/TBCLK	7	P4.7[(1)] (I/O)	I: 0; O: 1	0
		Timer_B3.TBCLK	0	1
		DV_{SS}	1	1

(1) Default after reset (PUC/POR)