2.7-V TO 5.5-V LOW POWER 10-BIT DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

SLAS259B – DECEMBER 1999 – REVISED APRIL 2004

features

- 10-Bit Voltage Output DAC
- Programmable Settling Time vs Power Consumption
  3 μs in Fast Mode
  9 μs in Slow Mode
- Ultra Low Power Consumption:
  900 μW Typ in Slow Mode at 3 V
  2.1 mW Typ in Fast Mode at 3 V
- Differential Nonlinearity ... <0.2 LSB Typ
- Compatible With TMS320 and SPI Serial Ports
- Power-Down Mode (10 nA)

- Buffered High-Impedance Reference Input
- Voltage Output Range ... 2 Times the Reference Input Voltage
- Monotonic Over Temperature
- Available in MSOP Package

applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

description

The TLV5606 is a 10-bit voltage output digital-to-analog converter (DAC) with a flexible 4-wire serial interface. The 4-wire serial interface allows glueless interface to TMS320, SPI, QSPI, and Microwire serial ports. The TLV5606 is programmed with a 16-bit serial string containing 4 control and 10 data bits. Developed for a wide range of supply voltages, the TLV5606 can operate from 2.7 V to 5.5 V.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. The settling time of the DAC is programmable to allow the designer to optimize speed versus power dissipation. The settling time is chosen by the control bits within the 16-bit serial input string. A high-impedance buffer is integrated on the REFIN terminal to reduce the need for a low source impedance drive to the terminal.

Implemented with a CMOS process, the TLV5606 is designed for single supply operation from 2.7 V to 5.5 V. The device is available in an 8-terminal SOIC package. The TLV5606C is characterized for operation from 0°C to 70°C. The TLV5606I is characterized for operation from −40°C to 85°C.

<table>
<thead>
<tr>
<th>T&lt;sub&gt;A&lt;/sub&gt;</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SMALL OUTLINE† (D)</td>
</tr>
<tr>
<td>0°C to 70°C</td>
<td>TLV5606CD</td>
</tr>
<tr>
<td>−40°C to 85°C</td>
<td>TLV5606ID</td>
</tr>
</tbody>
</table>

† Available in tape and reel as the TLV5606CDR, TLV5606IDR, TLV5606CDGKR, and the TLV5606IDGKR

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGND</td>
<td>5</td>
<td></td>
<td>Analog ground</td>
</tr>
<tr>
<td>CS</td>
<td>3</td>
<td>I</td>
<td>Chip select. Digital input used to enable and disable inputs, active low.</td>
</tr>
<tr>
<td>DIN</td>
<td>1</td>
<td>I</td>
<td>Serial digital data input</td>
</tr>
<tr>
<td>FS</td>
<td>4</td>
<td>I</td>
<td>Frame sync. Digital input used for 4-wire serial interfaces such as the TMS320 DSP interface.</td>
</tr>
<tr>
<td>OUT</td>
<td>7</td>
<td>O</td>
<td>DAC analog output</td>
</tr>
<tr>
<td>REFIN</td>
<td>6</td>
<td>I</td>
<td>Reference analog input voltage</td>
</tr>
<tr>
<td>SCLK</td>
<td>2</td>
<td>I</td>
<td>Serial digital clock input</td>
</tr>
<tr>
<td>VDD</td>
<td>8</td>
<td></td>
<td>Positive power supply</td>
</tr>
</tbody>
</table>
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (VDD to AGND) ................................. 7 V
Reference input voltage range ........................................ \( -0.3 \) V to \( V_{DD} + 0.3 \) V
Digital input voltage range ........................................ \( -0.3 \) V to \( V_{DD} + 0.3 \) V
Operating free-air temperature range, \( T_{A} \):
TLV5606C .................................................. \( 0^\circ \)C to 70°C
TLV5606I .................................................. \( -40^\circ \)C to 85°C
Storage temperature range, \( T_{stg} \) .................................... \( -65^\circ \)C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ........................ 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, VDD</td>
<td>VDD = 5 V</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VDD = 3 V</td>
<td>2.7</td>
<td>3</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>High-level digital input voltage, ( V_{IH} )</td>
<td>DVDD = 2.7 V</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>DVDD = 5.5 V</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low-level digital input voltage, ( V_{IL} )</td>
<td>DVDD = 2.7 V</td>
<td>0.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>DVDD = 5.5 V</td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Reference voltage, ( V_{ref} ) to REFIN terminal</td>
<td>VDD = 5 V (see Note 1)</td>
<td>AGND</td>
<td>2.048</td>
<td>VDD−1.5</td>
<td>V</td>
</tr>
<tr>
<td>Reference voltage, ( V_{ref} ) to REFIN terminal</td>
<td>VDD = 3 V (see Note 1)</td>
<td>AGND</td>
<td>1.024</td>
<td>VDD−1.5</td>
<td>V</td>
</tr>
<tr>
<td>Load resistance, ( R_{L} )</td>
<td></td>
<td>2</td>
<td>10</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>Load capacitance, ( C_{L} )</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Clock frequency, ( f_{CLK} )</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Operating free-air temperature, ( T_{A} )</td>
<td>TLV5606C</td>
<td>0</td>
<td>70</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>TLV5606I</td>
<td>−40</td>
<td>85</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

NOTE 1: Due to the x2 output buffer, a reference input voltage \( \geq V_{DD}/2 \) causes clipping of the transfer function.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

power supply

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply current, ( I_{DD} )</td>
<td>VDD = 5 V, VREF = 2.048 V, No load, All inputs = AGND or VDD, DAC latch = 0x800</td>
<td>Fast</td>
<td>0.9</td>
<td>1.35</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>VDD = 3 V, VREF = 1.024 V, No load, All inputs = AGND or VDD, DAC latch = 0x800</td>
<td>Fast</td>
<td>0.7</td>
<td>1.1</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slow</td>
<td>0.4</td>
<td>0.6</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slow</td>
<td>0.3</td>
<td>0.45</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Power down supply current (see Figure 12)</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply rejection ratio, ( PSRR )</td>
<td>Zero scale</td>
<td>See Note 2</td>
<td>−80</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>Full scale</td>
<td>See Note 3</td>
<td>−80</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power on threshold voltage, ( POR )</td>
<td></td>
<td>2</td>
<td>V</td>
</tr>
</tbody>
</table>

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying \( V_{DD} \) and is given by:
\[ PSRR = 20 \log \left( \frac{|E_{ZS}(V_{DD\max}) - E_{ZS}(V_{DD\min})|}{V_{DD\max}} \right) \]
3. Power supply rejection ratio at full scale is measured by varying \( V_{DD} \) and is given by:
\[ PSRR = 20 \log \left( \frac{|E_{G}(V_{DD\max}) - E_{G}(V_{DD\min})|}{V_{DD\max}} \right) \]
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

<table>
<thead>
<tr>
<th>static DAC specifications $R_L = 10 , \text{kΩ}, C_L = 100 , \text{pF}$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PARAMETER</strong></td>
</tr>
<tr>
<td>Resolution</td>
</tr>
<tr>
<td>INL Integral nonlinearity</td>
</tr>
<tr>
<td>DNL Differential nonlinearity</td>
</tr>
<tr>
<td>$E_{ZS}$ Zero-scale error (offset error at zero scale)</td>
</tr>
<tr>
<td>Zero-scale-error temperature coefficient</td>
</tr>
<tr>
<td>$E_G$ Gain error</td>
</tr>
<tr>
<td>Gain-error temperature coefficient</td>
</tr>
</tbody>
</table>

**NOTES:**
4. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors. Tested from code 10 to code 1023.
5. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code. Tested from code 10 to code 1023.
6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
7. Zero-scale-error temperature coefficient is given by: $E_{ZS\, TC} = \frac{E_{ZS}(T_{\text{max}}) - E_{ZS}(T_{\text{min}})}{V_{\text{ref}}} \times \frac{10^6}{(T_{\text{max}} - T_{\text{min}})}$.
8. Gain error is the deviation from the ideal output (2$V_{\text{ref}}$ - 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
9. Gain temperature coefficient is given by: $E_{G\, TC} = \frac{E_{G}(T_{\text{max}}) - E_{G}(T_{\text{min}})}{V_{\text{ref}}} \times \frac{10^6}{(T_{\text{max}} - T_{\text{min}})}$.

output specifications

<table>
<thead>
<tr>
<th><strong>PARAMETER</strong></th>
<th><strong>TEST CONDITIONS</strong></th>
<th><strong>MIN</strong></th>
<th><strong>TYP</strong></th>
<th><strong>MAX</strong></th>
<th><strong>UNIT</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_O$ Voltage output range</td>
<td>$R_L = 10 , \text{kΩ}$</td>
<td>0</td>
<td>AVDD-0.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output load regulation accuracy</td>
<td>$R_L = 2 , \text{kΩ}, , vs , 10 , \text{kΩ}$</td>
<td>0.1</td>
<td>±0.25</td>
<td>% of FS voltage</td>
<td></td>
</tr>
</tbody>
</table>

reference input (REF)

<table>
<thead>
<tr>
<th><strong>PARAMETER</strong></th>
<th><strong>TEST CONDITIONS</strong></th>
<th><strong>MIN</strong></th>
<th><strong>TYP</strong></th>
<th><strong>MAX</strong></th>
<th><strong>UNIT</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_I$ Input voltage range</td>
<td></td>
<td>0</td>
<td>VDD-1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$R_I$ Input resistance</td>
<td></td>
<td>10</td>
<td>MΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_I$ Input capacitance</td>
<td></td>
<td>5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference input bandwidth</td>
<td>REFIN = 0.2 $V_{pp}$ + 1.024 V dc</td>
<td>Slow</td>
<td>525</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Fast</td>
<td>1.3</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference feed through</td>
<td>REFIN = 1 $V_{pp}$ at 1 kHz + 1.024 V dc (see Note 10)</td>
<td></td>
<td>−75</td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE 10:** Reference feedthrough is measured at the DAC output with an input code = 0x000.

digital inputs

<table>
<thead>
<tr>
<th><strong>PARAMETER</strong></th>
<th><strong>TEST CONDITIONS</strong></th>
<th><strong>MIN</strong></th>
<th><strong>TYP</strong></th>
<th><strong>MAX</strong></th>
<th><strong>UNIT</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IH}$ High-level digital input current</td>
<td>$V_I = V_{DD}$</td>
<td></td>
<td>±1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$ Low-level digital input current</td>
<td>$V_I = 0 , \text{V}$</td>
<td></td>
<td>±1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$C_I$ Input capacitance</td>
<td></td>
<td>3</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

analog output dynamic performance

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_s(FS)</td>
<td>Output settling time, full scale</td>
<td>3</td>
<td>5.5</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>RL = 10 kΩ, See Note 11</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CL = 100 pF,</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fast</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Slow</td>
<td>9</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_s(CC)</td>
<td>Output settling time, code to code</td>
<td>1</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>RL = 10 kΩ, See Note 12</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CL = 100 pF,</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fast</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Slow</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew rate</td>
<td>3.6</td>
<td>V/µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RL = 10 kΩ, See Note 13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CL = 100 pF,</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fast</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Slow</td>
<td>0.9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Glitch energy</td>
<td>Code transition from 0x7FF to 0x800</td>
<td>10</td>
<td></td>
<td></td>
<td>nV−s</td>
</tr>
<tr>
<td>S/N</td>
<td>Signal to noise</td>
<td>62</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>S/(N+D)</td>
<td>Signal to noise + distortion</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
<td>–61</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>68</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

Notes:
11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x080 to 0x3FF or 0x3FF to 0x080. Not tested, ensured by design.
12. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of one count. Code change from 0x1FF to 0x200. Not tested, ensured by design.
13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

digital input timing requirements

| t_su(CS−FS)             | Setup time, CS low before FS↓   | 10  |     |     | ns   |
| t_su(FS−CK)             | Setup time, FS low before first negative SCLK edge | 8   |     |     | ns   |
| t_su(C16−FS)            | Setup time, sixteenth negative edge after FS low on which bit D0 is sampled before rising edge of FS | 10  |     |     | ns   |
| t_su(C16−CS)            | Setup time, sixteenth positive SCLK edge (first positive after D0 is sampled) before CS rising edge. If FS is used instead of the sixteenth positive edge to update the DAC, then the setup time is between the FS rising edge and CS rising edge. | 10  |     |     | ns   |
| t_wH                    | Pulse duration, SCLK high       | 25  |     |     | ns   |
| t_wL                    | Pulse duration, SCLK low        | 25  |     |     | ns   |
| t_su(D)                 | Setup time, data ready before SCLK falling edge | 8   |     |     | ns   |
| t_h(D)                  | Hold time, data held valid after SCLK falling edge | 5   |     |     | ns   |
| t_wH(FS)                | Pulse duration, FS high         | 20  |     |     | ns   |
PARAMETER MEASUREMENT INFORMATION

Figure 1. Timing Diagram
TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs LOAD CURRENT

3 V Slow Mode, SOURCE
V_{DD} = 3 V, V_{ref} = 1 V, Full Scale

3 V Fast Mode, SOURCE

Figure 2

OUTPUT VOLTAGE vs LOAD CURRENT

5 V Slow Mode, SOURCE
V_{DD} = 5 V, V_{ref} = 2 V, Full Scale

5 V Fast Mode, SOURCE

Figure 3

OUTPUT VOLTAGE vs LOAD CURRENT

3 V Slow Mode, SINK
V_{DD} = 3 V, V_{ref} = 1 V, Zero Code

3 V Fast Mode, SINK

Figure 4

OUTPUT VOLTAGE vs LOAD CURRENT

5 V Slow Mode, SINK
V_{DD} = 5 V, V_{ref} = 2 V, Zero Code

5 V Fast Mode, SINK

Figure 5
TYPICAL CHARACTERISTICS

**SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

![Graph showing supply current vs free-air temperature for different modes and supply voltages.](image)

**Figure 6**

**SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

![Graph showing supply current vs free-air temperature for different modes and supply voltages.](image)

**Figure 7**

**TOTAL HARMONIC DISTORTION vs FREQUENCY**

![Graph showing total harmonic distortion vs frequency for different modes and input conditions.](image)

**Figure 8**

**TOTAL HARMONIC DISTORTION vs FREQUENCY**

![Graph showing total harmonic distortion vs frequency for different modes and input conditions.](image)

**Figure 9**
TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION AND NOISE vs FREQUENCY

\[ V_{\text{ref}} = 1 \text{ V dc} + 1 \text{ V p/p Sinewave, Output Full Scale} \]

- THD: Total Harmonic Distortion

**Fast Mode**

```
THD - Total Harmonic Distortion And Noise - dB

0 5 10 20 30 50 100
f - Frequency - kHz
0 -80 -70 -60 -50 -40 -30 -20 -10
```

**Figure 10**

TOTAL HARMONIC DISTORTION AND NOISE vs FREQUENCY

\[ V_{\text{ref}} = 1 \text{ V dc} + 1 \text{ V p/p Sinewave, Output Full Scale} \]

- THD: Total Harmonic Distortion

**Slow Mode**

```
THD - Total Harmonic Distortion And Noise - dB

0 5 10 20 30 50 100
f - Frequency - kHz
0 -80 -70 -60 -50 -40 -30 -20 -10
```

**Figure 11**

SUPPLY CURRENT vs TIME (WHEN ENTERING POWER-DOWN MODE)

\[ I_{\text{DD}} = \text{Supply Current} - \mu\text{A} \]

```
I_{\text{DD}} - Supply Current - \mu\text{A}

0 100 200 300 400 500 600 700 800 900 1000
T - Time - ns
```

**Figure 12**
TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY ERROR

![Integral Nonlinearity Error Diagram](image)

Figure 13

DIFFERENTIAL NONLINEARITY ERROR

![Differential Nonlinearity Error Diagram](image)

Figure 14
general function

The TLV5606 is a 10-bit single supply DAC based on a resistor string architecture. The device consists of a serial interface, speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) is given by:

\[ \frac{2 \text{REF} \times \text{CODE}}{2^n} \text{[V]} \]

where \( \text{REF} \) is the reference voltage and \( \text{CODE} \) is the digital input value within the range of \( 0_{10} \) to \( 2^{n-1} \), where \( n = 10 \) (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the data format section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

Explanation of data transfer: First, the device has to be enabled with \( \overline{\text{CS}} \) set to low. Then, a falling edge of \( \text{FS} \) starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of \( \text{SCLK} \). After 16 bits have been transferred or \( \text{FS} \) rises, the content of the shift register is moved to the DAC latch which updates the voltage output to the new level.

The serial interface of the TLV5606 can be used in two basic modes:

- Four wire (with chip select)
- Three wire (without chip select)

Using chip select (four wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). The interface is compatible with the TMS320 family. Figure 15 shows an example with two TLV5606s connected directly to a TMS320 DSP.

![Figure 15. TMS320 Interface](image-url)
APPLICATION INFORMATION

serial interface (continued)

If there is no need to have more than one device on the serial bus, then CS can be tied low. Figure 16 shows an example of how to connect the TLV5606 to a TMS320, SPI, or Microwire port using only three pins.

![Diagram](image_url)

**Figure 16. Three-Wire Interface**

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to FS. If the word width is 8 bits (SPI and Microwire), two write operations must be performed to program the TLV5606. After the write operation(s), the DAC output is updated automatically on the next positive clock edge following the sixteenth falling clock edge.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

\[
\frac{1}{f_{SCLK\text{max}}} = \frac{1}{t_{WH(\text{min})} + t_{WL(\text{min})}} = 20 \text{ MHz}
\]

The maximum update rate is:

\[
\frac{1}{f_{UPDATE\text{max}}} = \frac{1}{16 \left( t_{WH(\text{min})} + t_{WL(\text{min})} \right)} = 1.25 \text{ MHz}
\]

The maximum update rate is a theoretical value for the serial interface, since the settling time of the TLV5606 has to be considered also.

data format

The 16-bit data word for the TLV5606 consists of two parts:

- Control bits \((D_{15} \ldots D_{12})\)
- New DAC value \((D_{11} \ldots D_{2})\)

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<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
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<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
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<tbody>
<tr>
<td>X</td>
<td>SPD</td>
<td>PWR</td>
<td>X</td>
<td>New DAC value (10 bits)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

X: don't care
SPD: Speed control bit. 1 → fast mode 0 → slow mode
PWR: Power control bit. 1 → power down 0 → normal operation

In power-down mode, all amplifiers within the TLV5606 are disabled.
TLV6506 interfaced to TMS320C203 DSP

Hardware Interfacing

Figure 17 shows an example how to connect the TLV5606 to a TMS320C203 DSP. The serial interface of the TLV5606 is ideally suited to this configuration, using a maximum of four wires to make the necessary connections. In applications where only one synchronous serial peripheral is used, the interface can be simplified even further by pulling CS low all the time as shown in the figure.

Figure 17. TLV5606 to DSP Interface

Software

No setup procedure is needed to access the TLV5606. The output voltage can be set using just a single command.

\[ \text{out data_addr, SDTR} \]

where data_addr points to an address location holding the control bits and the 12 data bits providing the output voltage data. SDTR is the address of the transmit FIFO of the synchronous serial port.

The following code shows how to use the timer of the TMS320C203 as a time base to generate a voltage ramp with the TLV5606.

A timer interrupt is generated every 205 \( \mu \)s. The corresponding interrupt service routine increments the output code (stored at 0x0064) for the DAC, adds the DAC control bits to the four most significant bits, and writes the new code to the TLV5606. The resulting period of the saw waveform is:

\[ \pi = 4096 \times 205 \times 10^{-6} \text{ s} = 0.84 \text{ s} \]
;*******************************************************************************************
;* Main Program
;*******************************************************************************************
    .ps 1000h
    .entry
start:
; disable interrupts
    setc INTM ; disable maskable interrupts
    splk #0ffffh, IFR
    splk #0004h, IMR

; set up the timer to interrupt ever 205uS
    splk #0000h, 60h
    splk #00FFh, 61h
    out 61h, PRD
    out 60h, TIM
    splk #0c2fh, 62h
    out 62h, TCR

; Configure SSP to use internal clock, internal frame sync and burst mode
    splk #0C008h, 63h
    out 63h, SSPCR
    splk #0CC3Eh, 63h
    out 63h, SSPCR
    splk #0000h, 64h ; set initial DAC value

; enable interrupts
    clrc INTM ; enable maskable interrupts

; loop forever!
next: idle ;wait for interrupt
    b next

; all else fails stop here
done: b done ;hang there

;***************************************************************************************
;* Interrupt Service Routines
;***************************************************************************************
INT1: ret ;do nothing and return
INT23: ret ;do nothing and return

TIM_ISR:
    lacl 64h ; restore counter value to ACC
    add #4h ; increment DAC value
    and #0FFCh ; mask 4 MSBs
    sacl 64h ; store 12 bit counter value
    or #4000h ; set DAC control bits
    sacl 65h ; store DAC value
    out 65h, SDTR ; send data
    clrc intm ; re-enable interrupts
    ret

.END
TLV5606 interfaced to MCS51® microcontroller

**hardware interfacing**

Figure 18 shows an example of how to connect the TLV5606 to an MCS51® compatible microcontroller. The serial DAC input data and external control signals are sent via I/O port 3 of the controller. The serial data is sent on the RxD line, with the serial clock output on the TxD line. P3.4 and P3.5 are configured as outputs to provide the chip select and frame sync signals for the TLV5606.

![Figure 18. TLV5606 to MCS51® Controller Interface](image)

**software**

The example program puts out a sine wave on the OUT pin.

The on-chip timer is used to generate interrupts at a fixed frequency. The related interrupt service routine fetches and writes the next sample to the DAC. The samples are stored in a lookup table, which describes one full period of a sine wave.

The serial port of the controller is used in mode 0, which transmits 8 bits of data on RxD, accompanied by a synchronous clock on TxD. Two writes concatenated together are required to write a complete word to the TLV5606. The CS and FS signals are provided in the required fashion through control of I/O port 3, which has bit addressable outputs.

```
;***********************************************************************
;* Title   : Ramp generation with TLV5606                              *
;* Version : 1.0                                                        *
;* MCU     : INTEL MCS51®                                              *
;* © (1998) Texas Instruments Incorporated                            *
;***********************************************************************

;------------------------------------------------------------------------
; Program function declaration
;------------------------------------------------------------------------

NAME GENSINE
MAIN SEGMENT CODE
ISR SEGMENT CODE
SINTBL SEGMENT CODE
VARI SEGMENT DATA
STACK SEGMENT IDATA

;------------------------------------------------------------------------
; Code start at address 0, jump to start
;------------------------------------------------------------------------

CSEG AT 0
```

MCS is a registered trademark of Intel Corporation
APPLICATION INFORMATION

LJMP start ; Execution starts at address 0 on power-up.

; Code in the timer0 interrupt vector

CSEG AT 0BH
LJMP timer0isr ; Jump vector for timer 0 interrupt is 000Bh

; Define program variables

RSEG VAR1
rolling_ptr: DS 1

; Interrupt service routine for timer 0 interrupts

RSEG ISR
timer0isr:
PUSH PSW
PUSH ACC
CLR T0 ; set CSB low
CLR T1 ; set FS low

; The signal to be output on the dac is a sine function. One cycle of a sine wave is
; held in a table @ sinevals as 32 samples of msb, lsb pairs (64 bytes). The pointer,
; rolling_ptr, rolls round the table of samples incrementing by 2 bytes (1 sample) on
; each interrupt (at the end of this routine).

MOV DPTR,#sinevals ; set DPTR to the start of the table of sine signal values
MOV A,rolling_ptr ; ACC loaded with the pointer into the sine table
MOVC A,@A+DPTR ; get msb from the table
ORL A, #00H ; set control bits
MOV SBUF,A ; send out msb of data word

MOVA,rolling_ptr; move rolling pointer in to ACC
INC A ; increment ACC holding the rolling pointer
MOV A,@A+DPTR ; which is the lsb of this sample, now in ACC

MSB_TX:
JNB TI, MSB_TX ; wait for transmit to complete
CLR TI ; clear for new transmit
MOV SBUF,A ; and send out the lsb

LSB_TX:
JNB TI, LSB_TX ; wait for lsb transmit to complete
SETB T1 ; set FS = 1
CLR TI ; clear for new transmit

MOV A,rolling_ptr ; load ACC with rolling pointer
INC A ; increment the ACC twice, to get next sample
INC A
ANL A,#03FH ; wrap back round to 0 if >64
MOV rolling_ptr,A ; move value held in ACC back to the rolling pointer
SETB T0 ; CSB high
POP ACC
POP PSW

RETI

; Set up stack


APPLICATION INFORMATION

RSEG STACK
DS 10h ; 16 Byte Stack!

; -- Main Program --

RSEG MAIN

start:
  MOV SP,#STACK-1 ; first set Stack Pointer
  CLR A
  MOV SCON,A ; set serial port 0 to mode 0
  MOV TMOD,#02H ; set timer 0 to mode 2 - auto-reload
  MOV TH0,#0C8H ; set TH0 for 16.67 kHs interrupts
  SETB T1 ; set FS = 1
  SETB T0 ; set CSB = 1
  SETB ET0 ; enable timer 0 interrupts
  SETB EA ; enable all interrupts
  MOV rolling_ptr,A ; set rolling pointer to 0
  SETB TR0 ; start timer 0

always:
  SJMP always ; while(1) !

RET

; -- Table of 32 sine wave samples used as DAC data --

RSEG SINTBL

sinevals:
  DW 01000H
  DW 0903CH
  DW 05094H
  DW 0305CH
  DW 0B084H
  DW 0F0C8H
  DW 0F0E0H
  DW 0F038H
  DW 0F06CH
  DW 0F0E0H
  DW 0B084H
  DW 0305CH
  DW 05094H
  DW 0903CH
  DW 01000H
  DW 06020H
  DW 0A0E8H
  DW 0C060H
  DW 040F8H
  DW 080B4H
  DW 0009CH
  DW 00050H
  DW 00024H
  DW 00050H
  DW 0009CH
  DW 080B4H
  DW 040F8H
  DW 0C060H
  DW 0A0E8H
  DW 06020H

END
APPLICATION INFORMATION

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 19.

![Figure 19. Effect of Negative Offset (Single Supply)](image)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane, making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1-µF ceramic-capacitor bypass should be connected between VDD and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 20 shows the ground plane layout and bypassing technique.

![Figure 20. Power-Supply Bypassing](image)
definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (Ezs)

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (EG)

Gain error is the error in slope of the DAC transfer function.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
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</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
(3) **MSL, Peak Temp.** -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL BOX INFORMATION**

### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width**

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**
- **Pocket Quadrants**

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<th>Pins</th>
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</table>
### Tape and Reel Box Dimensions

<table>
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<tr>
<th>Device</th>
<th>Package</th>
<th>Pins</th>
<th>Site</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV5606CDGKR</td>
<td>DGK</td>
<td>8</td>
<td>SITE 60</td>
<td>346.0</td>
<td>346.0</td>
<td>29.0</td>
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<tr>
<td>TLV5606CDR</td>
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<td>TLV5606IDGKR</td>
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<td>TLV5606IDR</td>
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<td>SITE 60</td>
<td>346.0</td>
<td>346.0</td>
<td>29.0</td>
</tr>
</tbody>
</table>
DGK (S—PDSO—G8)  PLASTIC SMALL—OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (.15) per end.
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed .017 (.43) per side.
E. Reference JEDEC MS-012 variation AA.
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