ABSTRACT

This document describes issues of interest related to migration from the Texas Instruments TMS320C6211B/C6711B GFN package to the TMS320C6713 digital signal processor (DSP) GDP package. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the device data sheets. Migration issues from C6211B/C6711B to C6713 are indicated with the following symbols, which are included at the beginning of each section:

[H] Means hardware modification is required.

[S] Means system/software modification is required.

[D] Means the C6211B/C6711B and C6713 are different (usually due to added features on the C6713), but no modification is necessary for migration (that is, the devices are different but compatible).

With detailed description in this document, migration and development of C6713 systems can be accomplished with ease.
1 Core Power [H]

The core voltage of C6713 is now 1.26 V with 5% tolerance; down from 1.8 V on the C6211B/C6711B and 1.9 V on the C6711. The power supply circuit on the board needs to be modified to support this.

2 Package and Pins [H, S]

The GDP package of the C6713 has 272 pins. The GDP package is very similar to the C6211B/C6711B’s 256-pin GFN package, plus the addition of 16 ground thermal pins in the middle. The mechanics of the GDP package is also slightly different. Refer to Appendix A for C6713-GDP mechanical specifications.

2.1 CLKOUT1 Pin no Longer Exists [H, S]

The CLKOUT1 pin does not exist on the C6713. The D7 pin that is the CLKOUT1 pin on the C6211B/C6711B now becomes a reserved, no-connect pin on the C6713.

2.2 Connect Pin Y20 to GROUND [H]

This pin is a reserved pin on the C6211B/C6711B. This pin must be connected to GROUND on the C6713.

2.3 Pullup CLKS1/SCL1 (E1) and DR1/SDA1 (M2) Pins [H]

The McBSP1/I2C1 pins E1 and M2 on the C6713 do not have internal pullup/down resistors. These pins must be externally pulled up.

2.4 EMU2 Pin Location Change [H]

The EMU2 pin location is changed from D10 (now CLKOUT3) to D3 (was reserved, no-connect). This EMU2 pin is unused, so it should not pose any implication.
2.5 **Pullup Pins N1 and N2 [H]**

Pin N1 is a DVDD pin on the C6211B/C6711B, and pin N2 is a reserved, no-connect pin. On the C6713, these are I2C0 pins and must be pulled up with external resistors.

2.6 **Pulldown Pin D12 [H]**

Pin D12 is a reserved, no-connect pin on the C6211B/6711B. On the C6713, this reserved pin must be pulled down with an external resistor for proper device operation.

2.7 **Pins B11 and A12 are Now Reserved [H]**

Pins B11 and A12 are connected to VSS and VDD, respectively, on C6211B/C6711B. These pins are reserved (unconnected) on C6713.

2.8 **Internal/External Pull Resistors [H]**

For C6713, the recommended external pullup and pulldown resistors used to oppose the internal pull should not be greater than 4.4 kΩ and 2.0 kΩ, respectively. This is compatible with the recommended C6211B/C6711B external pullup and pulldown resistor values (1 kΩ). However, the internal pullup (IPU) and internal pulldown (IPD) value for C6713 is now 18 kΩ (approximate) and 13 kΩ (approximate), respectively. For C6211B/C6711B, both the IPU and IPD are 30 kΩ.

3 **PLL and PLL Controller [H, S, D]**

The PLL controller is a new peripheral on C6713. In addition to a new software programmable PLL, it also includes a reset controller, plus a set of software programmable pre-scalers and post-dividers. See the *TMS320C6000 PLL Controller Peripheral Reference Guide* (SPRU233) for details on this peripheral. Also see the C6713 data sheet for the PLL circuit and other device-specific PLL information.

3.1 **In PLL Mode, External PLL Components/Circuit Must be Modified [H, PLL Mode Only]**

The new PLL on the C6713 requires a new external PLL circuit. Pin C5 is now the analog 3.3-V power pin (PLLHV) for the C6713 PLL. The PLL pins on the C6211B/C6711B, which are A4, C6, and B5 now, become CVDD, GROUND, and Reserved (no-connect), respectively. For details on the external PLL circuit, see the device-specific data sheet.

In bypass mode, the PLL circuit is still required. However, regardless of bypass or PLL mode, the PLL controller peripheral must be programmed to generate desired clocks.

3.2 **CLKMODE0 Pin Must Always be Pulled High [H, S]**

The CLKMODE0 pin definition is now changed. On the C6211B/C6711B, the CLKMODE0 selects between x1 and x4 PLL mode. On the C6713, the CLKMODE0 pin must always be pulled high (default). Therefore, if the existing board is in PLL bypass mode (CLKMODE=0), the pulldown resistor must be removed to set CLKMODE=1 (default due to internal pullup resistor). The PLL Controller registers must then be programmed in software to the desired PLL mode and clock frequencies.
3.3 Reset Timing [S, D]

The PLL controller on the C6713 has a reset controller logic that internally lengthens the reset signal, to ensure that input clocks are stable before internal reset is released. See the Reset Timing section of the data sheet, *TMS320C6711, TMS320C6711B, TMS320C6711C Floating-Point Digital Signal Processors* (SPRS088) and the *TMS320C6000 DSP Phase-Locked Loop (PLL) Controller Peripheral Reference Guide* (SPRU233). The following is affected by the difference in C6713 reset timing:

- **Pin states during reset [S]**
  During the reset sequence, the states of clocks and other pins are slightly different from those of the C6211B/C6711B

- **HPI boot mode [S]**
  If the HPI boot mode is enabled (HD[4:3] = 00b), the host must wait until reset is released internally before starting boot load. Furthermore, the C6713 device comes up in bypass mode by default out of reset; therefore, the clock rate is initially slow. When migrating from an existing system, the host needs to take into account that the device is initially in bypass mode. It may be necessary for the host to slow down the HPI interface, to insure that the slower DSP can recognize the host commands.

- **EMIF boot mode [D]**
  If the EMIF boot mode is employed, then no change is needed. The EMIF boot will start automatically after the internal reset signal is released.

4 New EKSR and EKEN Register Bits [S, D]

The EKSR bit in the DEVCFG register selects EMIF input clock source between the internal clock, SYSCLK3 (default), and ECLKIN.

- **EKSR = 0**: EMIF input clock is SYSCLK3 (default).
- **EKSR = 1**: EMIF input clock is ECLKIN.

The SYSCLK3 frequency is software-programmable via PLLDIV3 register in the PLL controller peripheral.

For existing systems using ECLKIN, EKSR should be set to 1 in order to use ECLKIN. If SYSCLK3 (default) is desired, PLLDIV3 must be set to the desired clock rate prior to any EMIF accesses.

The ECLKOUT pin on the C6211B/C6711B is always running as long as the EMIF input clock source ECLKIN is supplied. On C6713, the EKEN bit is added to the EMIF global control register to enable or disable ECLKOUT. The EKEN bit functions as follows:

- **EKEN=0**: ECLKOUT held low
- **EKEN=1**: ECLKOUT enabled to clock (default)
5 **New General-Purpose Input/Output (GPIO) Module With 5 Pins (GP[7:4, 2]) [S, D]**

In order to use these pins as GPIO pins, the GPxEN bits in the GPIO Enable Register (GPEN) and the GPxDIR bits in the GPIO Direction Register (GPDIR) must be properly configured, where x is 7, 6, 5, 4, or 2.

- GPxEN = 1: GPx pin enabled
- GPxDIR = 0: GPx pin is an input
- GPxDIR = 1: GPx pin is an output

5.1 **EXT_INT4–7 are Now GP4–7 [S, D]**

External interrupts 4–7 now go through the GPIO module. When these pins are used as interrupt inputs, the GP4–7 must be configured to be inputs (in GPDIR register) and enabled (in GPEN register), in addition to enabling the interrupts in the Interrupt Enable Register (IER).

5.2 **GP2 Pin is Muxed With CLKOUT2 Pin [D]**

The GP2 pin is multiplexed with the CLKOUT2 pin; default is CLKOUT2. In order to use this pin as GPIO pin (GP2), the GPxEN bits in the GPEN register and the GPxDIR bits in the GPDIR register must be properly configured.

6 **Power-Down Modes [H, S]**

The power-down modes, PD2 and PD3, operation differs for the C6713 device in bypass mode. When bypassing the PLL, the device still receives clocks from the external clock input. PD2 and PD3 is only effective in PLL mode. See the *TMS320C6713 Digital Signal Processor Silicon Errata (Silicon Revision 1.1)* (SPRZ191) for more details.

7 **Boundary Scan Mode [H]**

For the Boundary Scan mode, the RESET pin needs to be driven low for the C6713 device. This is not a requirement for C6211B/C6711B.

8 **AC Timings [H, S]**

To view the differences in AC timings, see the device-specific data sheet.

9 **Pin Migration Summary**

Table 1 summarizes all the pin-related modifications needed when migrating from C6211B/C6711B to C6713.
Table 1. Pin Migration Summary

<table>
<thead>
<tr>
<th>Pin</th>
<th>C6211B/C6711B</th>
<th>C6713</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7</td>
<td>CLKOUT1</td>
<td>Reserved</td>
</tr>
<tr>
<td>Y20</td>
<td>Reserved, no-connect</td>
<td>GROUND</td>
</tr>
<tr>
<td>C5</td>
<td>DVDD</td>
<td>PLLHV. Analog 3.3-V power for PLL.</td>
</tr>
<tr>
<td>A4</td>
<td>PLL analog Vcc connection</td>
<td>CVDD</td>
</tr>
<tr>
<td>C6</td>
<td>PLL analog GND connection</td>
<td>GROUND</td>
</tr>
<tr>
<td>B5</td>
<td>PLL low-pass filter connection to external components</td>
<td>Reserved, no-connect</td>
</tr>
<tr>
<td>E1 and M2</td>
<td>Have IPD, IPU; respectively</td>
<td>No IPU/IPD. Must be externally pulled up.</td>
</tr>
<tr>
<td>D10</td>
<td>EMU2</td>
<td>CLKOUT3</td>
</tr>
<tr>
<td>D3</td>
<td>Reserved, no-connect</td>
<td>EMU2</td>
</tr>
<tr>
<td>N1</td>
<td>DVDD</td>
<td>I2C0 pins. Must be externally pulled up.</td>
</tr>
<tr>
<td>N2</td>
<td>Reserved, no-connect</td>
<td></td>
</tr>
<tr>
<td>D12</td>
<td>Reserved, no-connect</td>
<td>Must be externally pulled down.</td>
</tr>
<tr>
<td>B11</td>
<td>Vss</td>
<td>Reserved, no-connect</td>
</tr>
<tr>
<td>A12</td>
<td>CVDD</td>
<td>Reserved, no-connect</td>
</tr>
</tbody>
</table>

NOTE: Do not oppose the IPU/IPD settings of non-configuration HD pins (HD[15:9, 7:5, 2:0]).

10 New/Enhanced Peripherals [D]

The C6713 DSP features new or enhanced peripherals over the C6211B/C6711B. These include:

- **Larger L2 SRAM**
  The SRAM size of the L2 memory on C6713 DSP has been increased by 192K bytes, bringing the total L2 size to 256K bytes. Of 256K bytes total, 64K bytes are programmable to be L2 cache or SRAM, while the other 192K bytes are SRAM only.

- **PLL and PLL Controller**
  The multiplier factor of the PLL on C6713 DSP is programmable to be x4, x5, up to x25. In addition to the new PLL, the C6713 also features the PLL Controller peripheral. The PLL Controller is a flexible, programmable clock generator, capable of generating DSP core clock, CLKOUT3, EMIF and other peripheral clocks. See section 3 for migration issues regarding this peripheral.

- **General-Purpose Input/Output (GPIO)**
  The C6713 has a dedicated GPIO module consisting of 16 pins. The GPIO module can be programmed to generate CPU interrupts and EDMA events.

- **Multichannel Audio Serial Port (McASP)**
  The C6713 has two McASP modules. Each of the McASPs features two independent clock zones (for transmit and receive) and 8 data pins. The McASP supports data interface in Time-Division Multiplexed (TDM) format, burst format, and Digital Audio Interface Transmit (DIT) format, where the bit stream is encoded for S/PDIF, AES-3, IEC-60958 transmissions.
• Inter-Integrated Circuit (I2C) Port

The C6713 has two I2C ports. Each of them is capable of transmitting and receiving in both master and slave interfaces.

Note that some peripheral pins are multiplexed with other pins. This means that some peripherals cannot be used with others. See the device data sheet for detailed information on available device configurations.

See also *How to Begin Development Today with The TMS320C6713 Floating-Point DSP* (SPRA809) for details on differences between the C6711B and the C6713 DSPs.

11 References

4. *How to Begin Development Today With the TMS320C6713 Floating-Point DSP* (SPRA809).
Appendix A  GDP (S-PBGA-N272) Plastic Ball Grid Array

NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC MO-151
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Mailing Address:
Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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